

SLM50N06T

60V N-Channel MOSFET

General Description

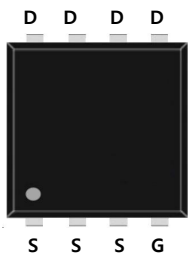
This Power MOSFET is produced using Msemitek's advanced TRENCH technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

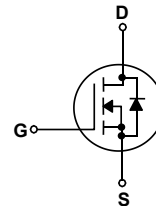
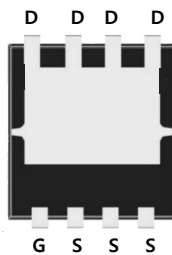
- PWM Application
- Load Switch
- Power Management

Features

- 50A, 60V, $R_{DS(on)Typ} = 14.8m\Omega @ V_{GS} = 10V$
 $R_{DS(on)Typ} = 18.2m\Omega @ V_{GS} = 4.5V$
- Low gate charge (typical 27.2nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



DFN5*6



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLM50N06T	Units
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	50	A
	- Continuous ($T_C = 100^\circ\text{C}$)	33	A
I_{DM}	Drain Current - Pulsed (Note 1)	200	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	68	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	39	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.31	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD50N06A	SLD50N06A	D-Pak	Tape & Reel	2500	25000

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	2.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	--	13	17	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	--	17	22	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2155	--	pF
C_{oss}	Output Capacitance		--	101	--	pF
C_{riss}	Reverse Transfer Capacitance		--	92	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 30\text{ A},$ $R_G = 1.8\text{ }\Omega, V_{GS} = 10\text{ V}$ (Note 3)	--	6	--	ns
t_r	Turn-On Rise Time		--	4.5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	24	--	ns
t_f	Turn-Off Fall Time		--	5	--	ns
Q_g	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 30\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3)	--	46	--	nC
Q_{gs}	Gate-Source Charge		--	6	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC
R_G	Gate Resistance	$f = 1\text{ MHz}$	--	3.5	--	Ω

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	50	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	200	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	--	--	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 30\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	25	--	ns
Q_{rr}	Reverse Recovery Charge		--	35	--	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ\text{C}, V_{DD} = 20\text{ V}, V_G = 10\text{ V}, R_G = 25\text{ }\Omega, L = 0.5\text{ mH}$,
3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 0.5\%$

N- Channel Typical Characteristics

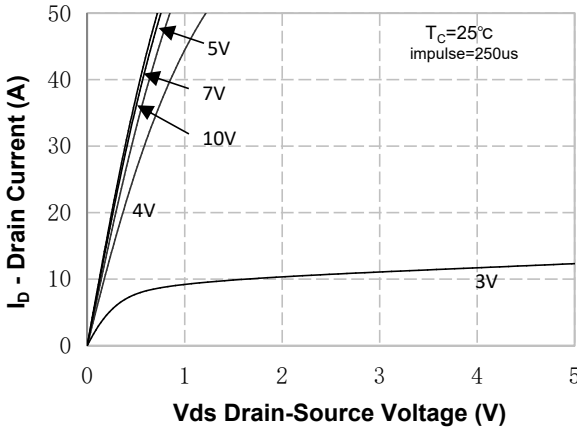


Figure 1. On-Region Characteristics

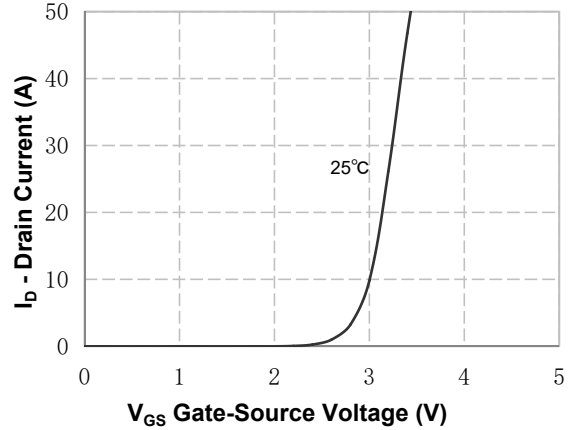


Figure 2. Transfer Characteristics

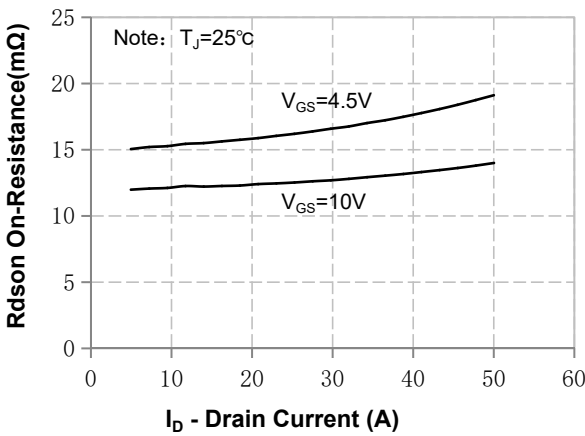


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

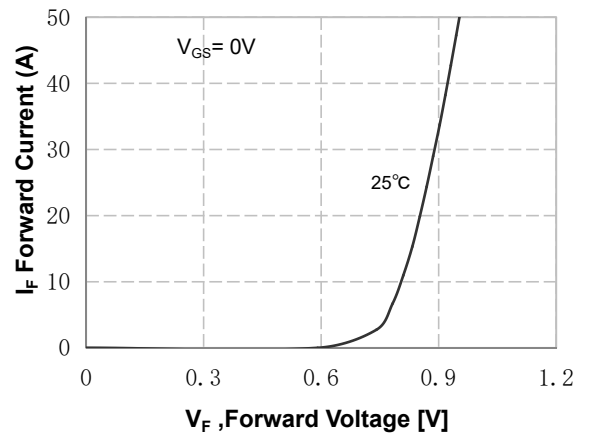


Figure 4. Body Diode Forward Voltage Variation with Source Current

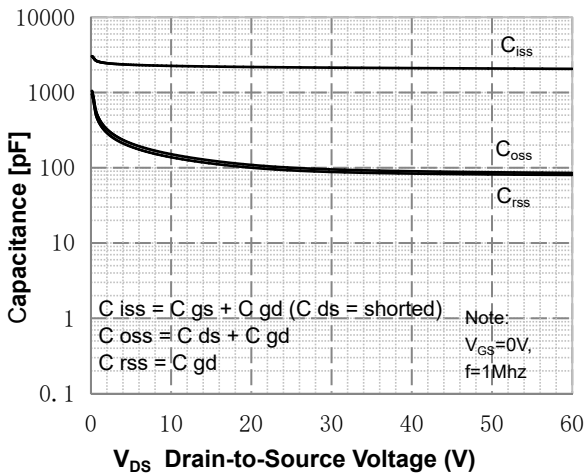


Figure 5. Capacitance Characteristics

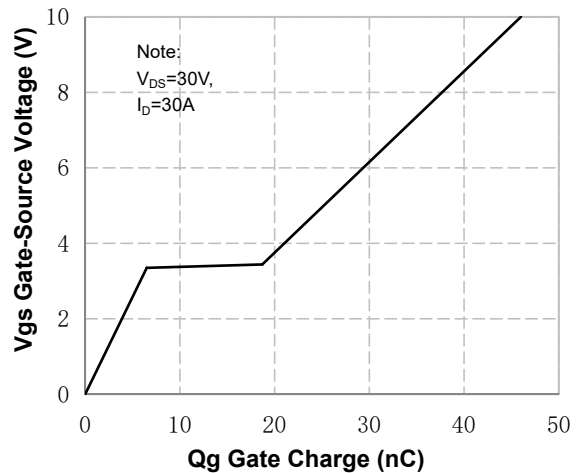


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

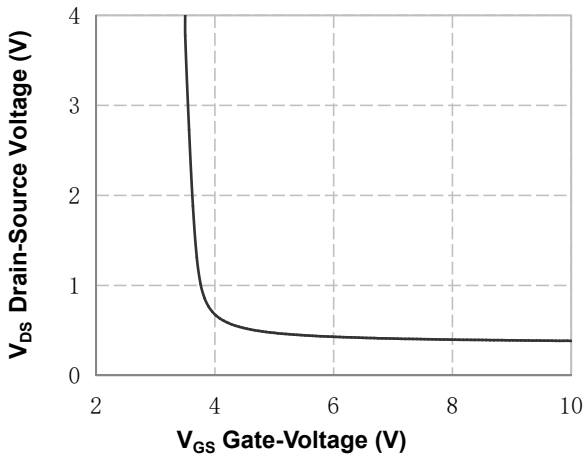


Figure 7. V_{DS} Drain-Source Voltage vs Gate Voltage

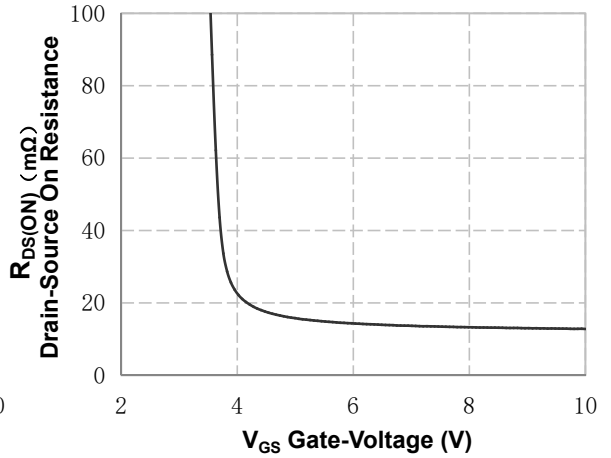


Figure 8. On-Resistance vs Gate Voltage

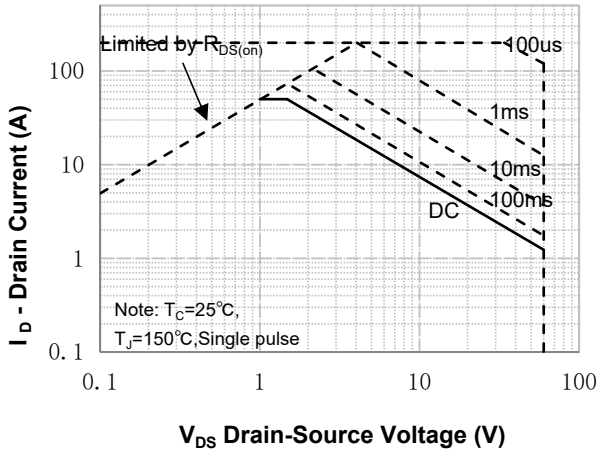


Figure 9. Maximum Safe Operating Area

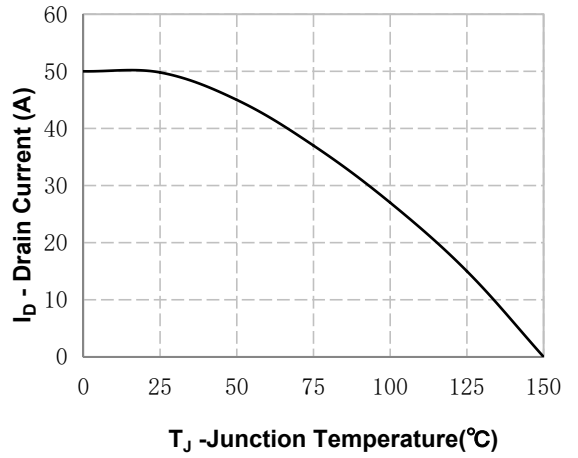


Figure 10. Maximum Continuous Drain Current vs Temperature

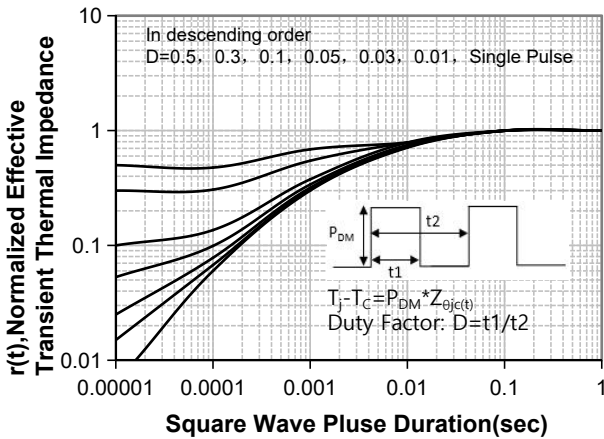
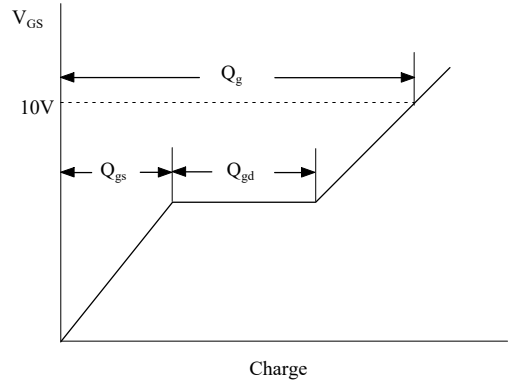
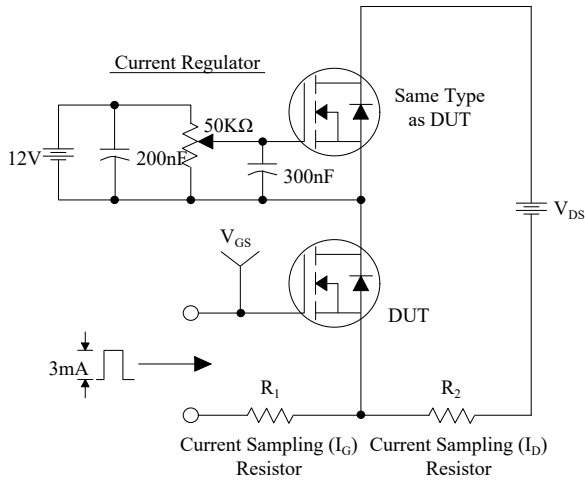
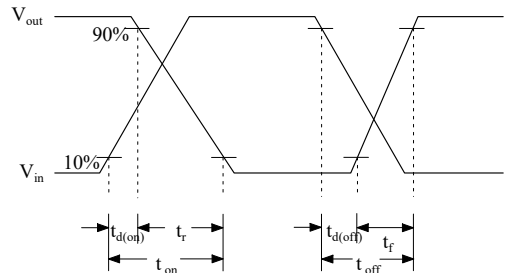
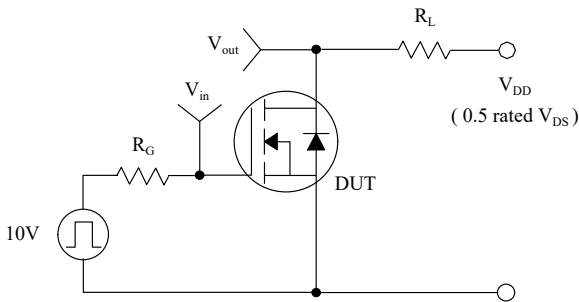


Figure 11. Transient Thermal Response Curve

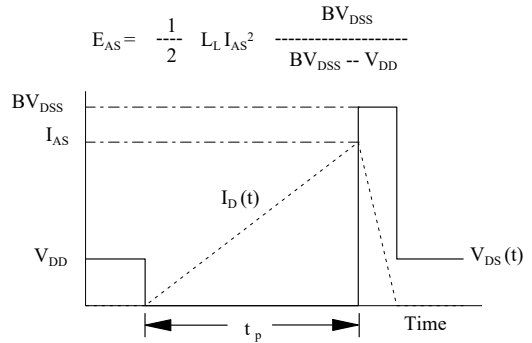
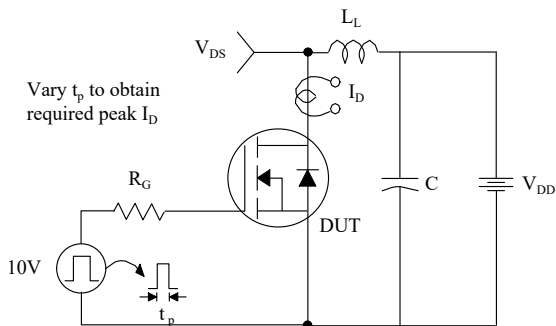
Gate Charge Test Circuit & Waveform



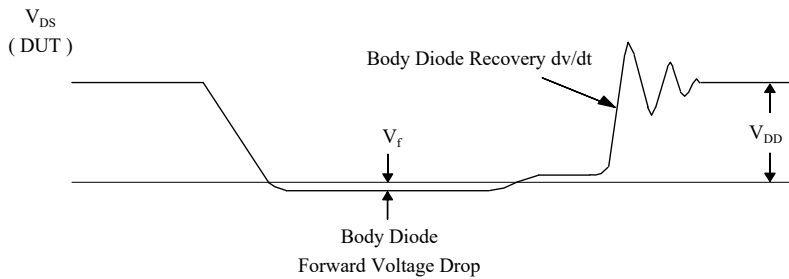
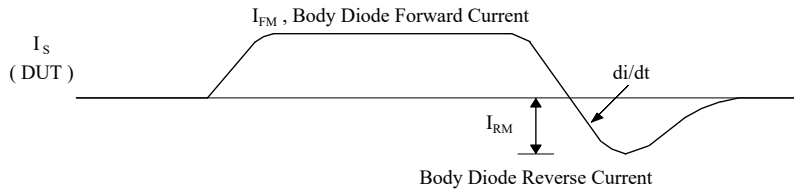
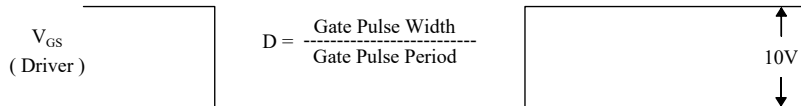
Resistive Switching Test Circuit & Waveforms



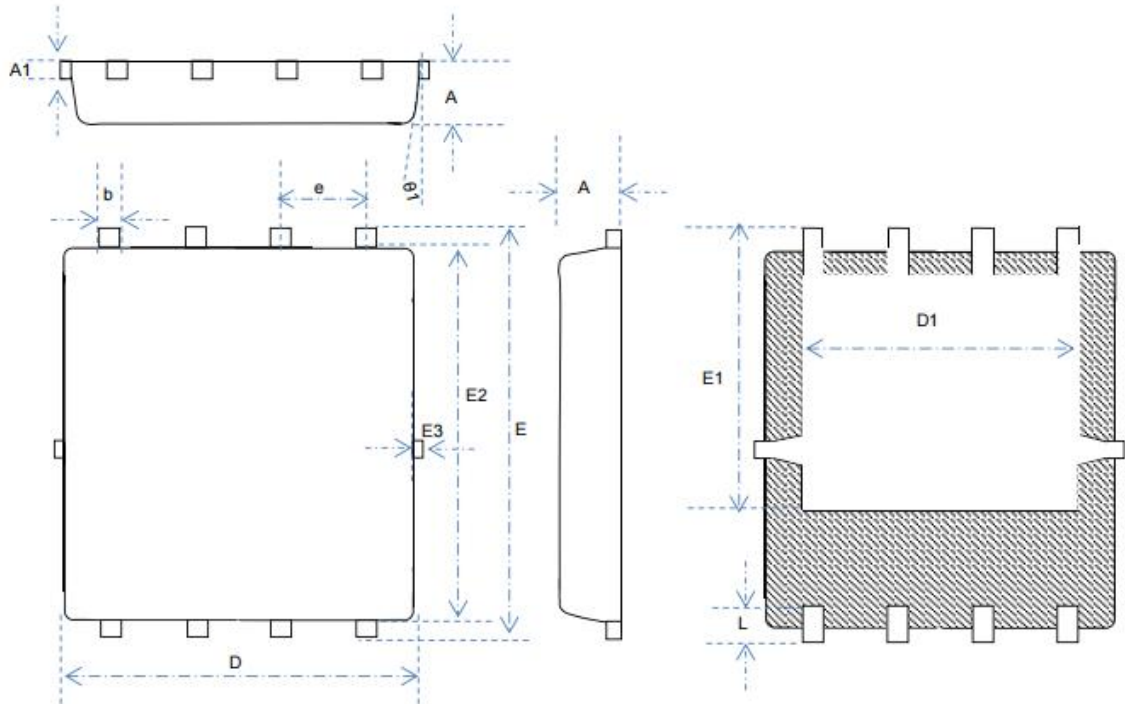
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



DFN 5*6 OUTLINE



SYMBOL	Mechanical Dimensions/mm			SYMBOL	Mechanical Dimensions/mm		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.85	0.95	1.05	D	5.10	5.20	5.30
A1	0.254 REF			e	1.270 TYPE		
b	-	0.30	-	D1	3.90	4.0	4.10
E	5.85	6.05	6.25	L	0.54	0.64	0.74
E1	3.90	4.10	4.30				
E2	5.45	5.55	5.65	θ1	8°	10°	12°
E3	-	-	0.15				

NAME	DFN 5*6 OUTLINE	UNIT	mm	DESIGNED	Shawn	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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