SLN50P03T
-30V P -Channel MOSFET

General Description

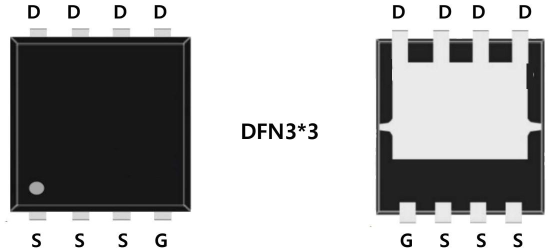
This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

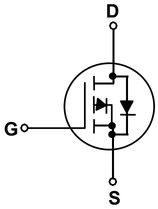
Features

- P-Channel: -30V -50A
  $R_{DS(on)Typ}$=9.2mΩ@V_{GS} = -10 V
  $R_{DS(on))Typ}$= 12.5mΩ@V_{GS} = -4.5V
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Application

☑ PWM Application
☑ Load Switch
☑ Power Management





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLN50P03T	Units
V_{DSS}	Drain-Source Voltage	-30	V
I_D	Drain Current - Continuous (T_C = 25℃)	-50	A
	- Continuous (T_C = 100℃)	-33	A
I_{DM}	Drain Current - Pulsed (Note 1)	-200	A
V_{GSS}	Gate-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy	225	mJ
P_D	Power Dissipation (T_C = 25℃)	20	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.25	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLN50P03T	SLN50P03T	DFN3*3	Tape & Reel	5000	50000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 uA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -30 V, V_{GS} = 0 V	--	--	-1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20V, V_{DS} = 0 V	--	--	-100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 uA	-1.0	-1.5	-2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -12A	--	9.2	12	mΩ
		V_{GS} = -4.5 V, I_D = -7A	-	12.5	17	

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	--	1770	-	pF
C_{oss}	Output Capacitance		--	231	-	pF
C_{rss}	Reverse Transfer Capacitance		--	216	-	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= -10 V, V_{DS}= -15V, R_G = 3 Ω ,I_D= -25A	--	13	--	ns
t_r	Turn-On Rise Time		--	8.5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	26	--	ns
t_f	Turn-Off Fall Time		--	12	--	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -25A, V_{GS} = -10V	--	32	--	nC
Q_{gs}	Gate-Source Charge		--	6	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	-50	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-200	A
V_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =-10A,T J = 25℃	--	--	-1.2	V
t_{rr}	Reverse Recovery Time T J = 25°C, IF =-25A,di/dt =100A/μs	--	32	-	nS
Q_{rr}	Reverse Recovery Charge T J = 25°C, IF =-25A,di/dt =100A/μs	--	21	-	nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T J =25℃, VDD =-20V, VG =-10V, L=0.5mH.
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

P- Channel Typical Characteristics

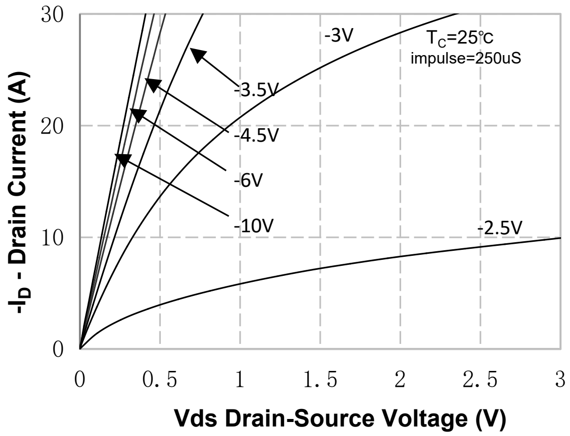


Figure 1. On-Region Characteristics

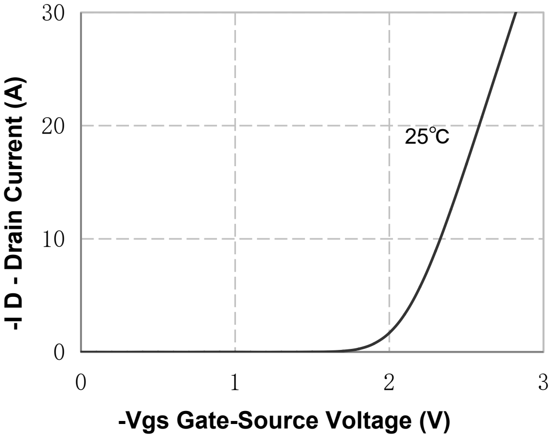


Figure 2. Transfer Characteristics

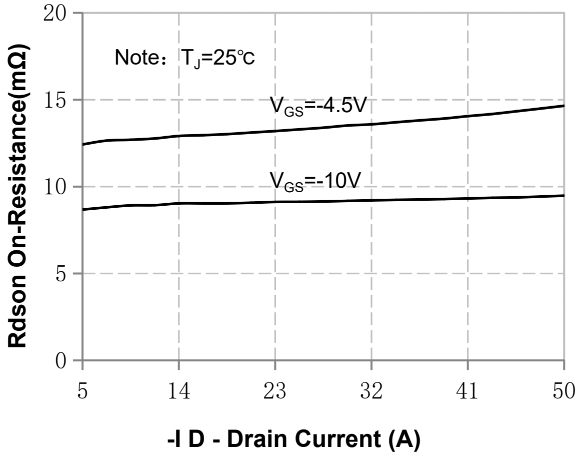


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

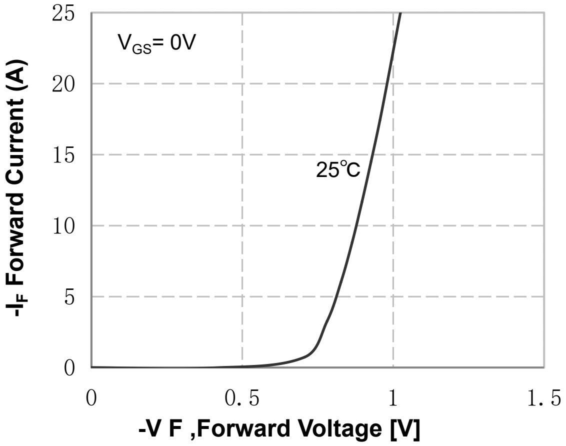


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

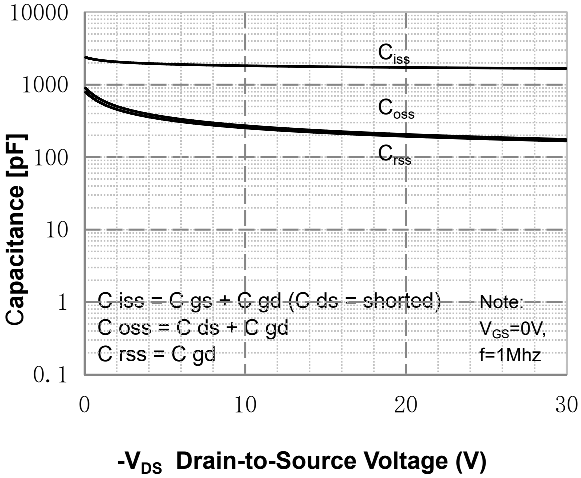


Figure 5. Capacitance Characteristics

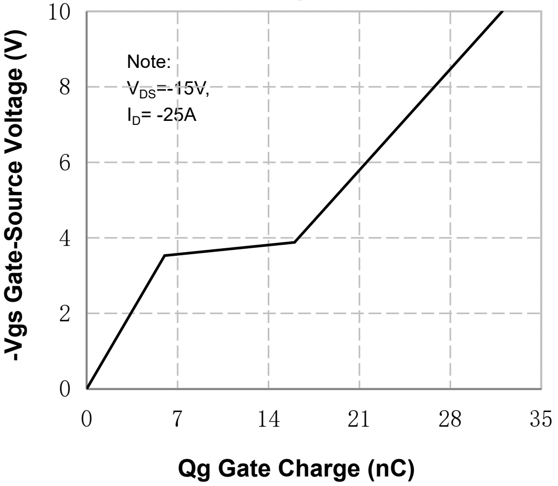
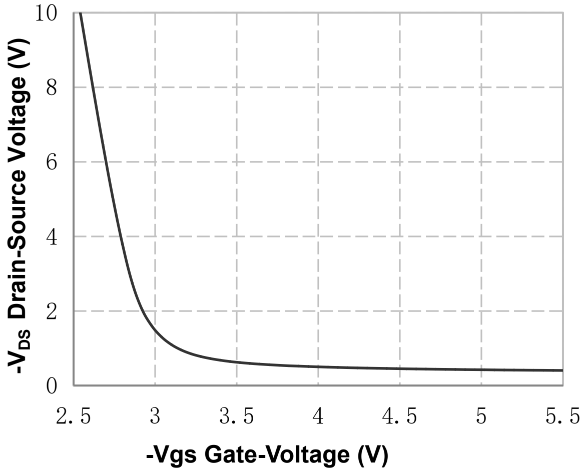


Figure 6. Gate Charge Characteristics

P- Channel Typical Characteristics (Continued)



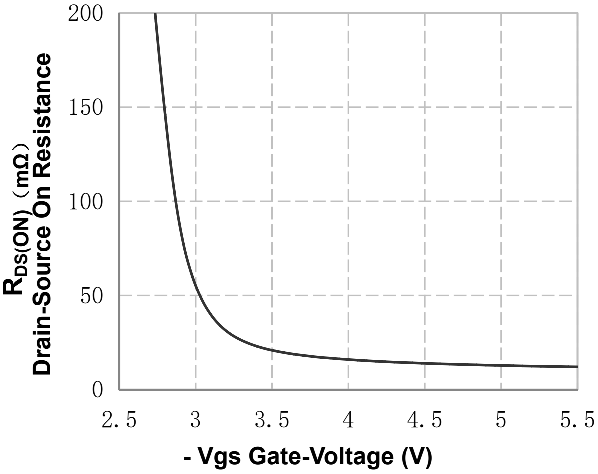


Figure 7. V_{DS} Drain-Source Voltage vs Gate Voltage

Figure 8. On-Resistance vs Gate Voltage

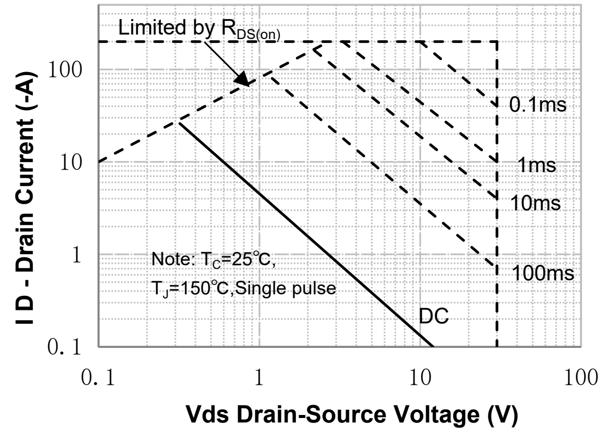


Figure 9. Maximum Safe Operating Area

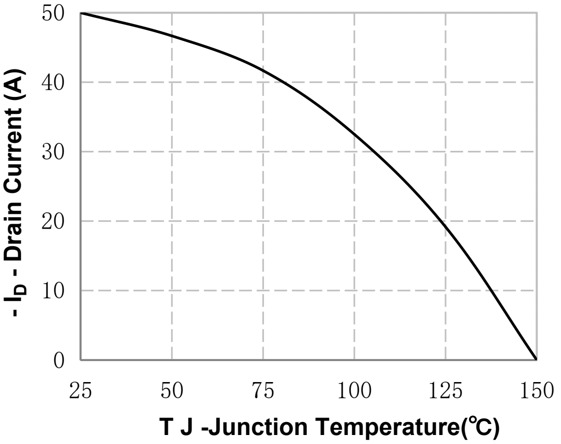


Figure 10. Maximum Continuous Drain Current vs Temperature

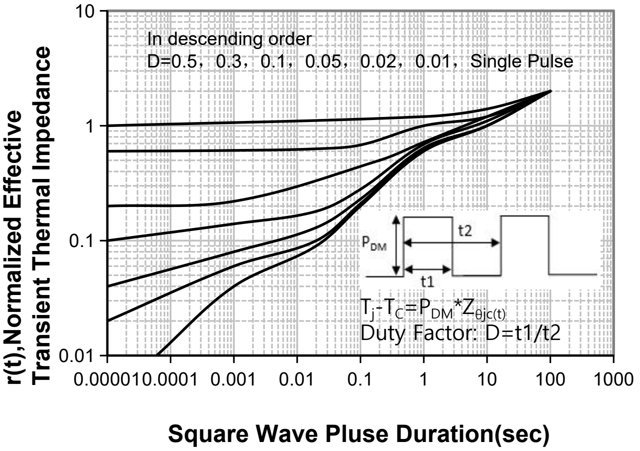
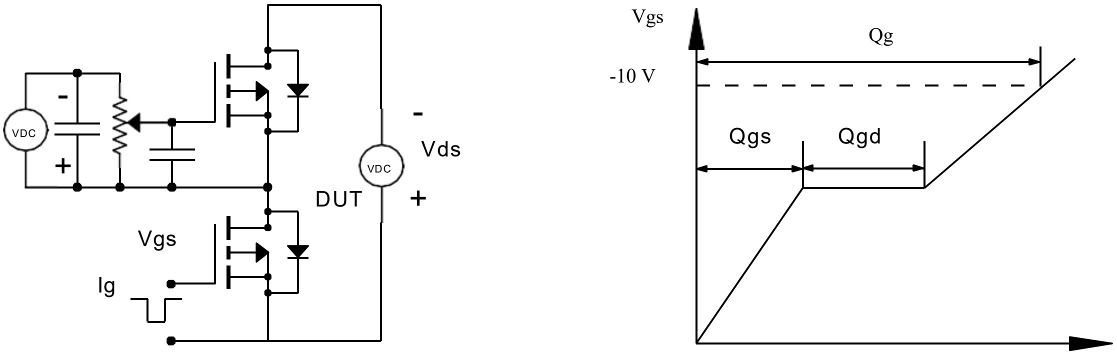


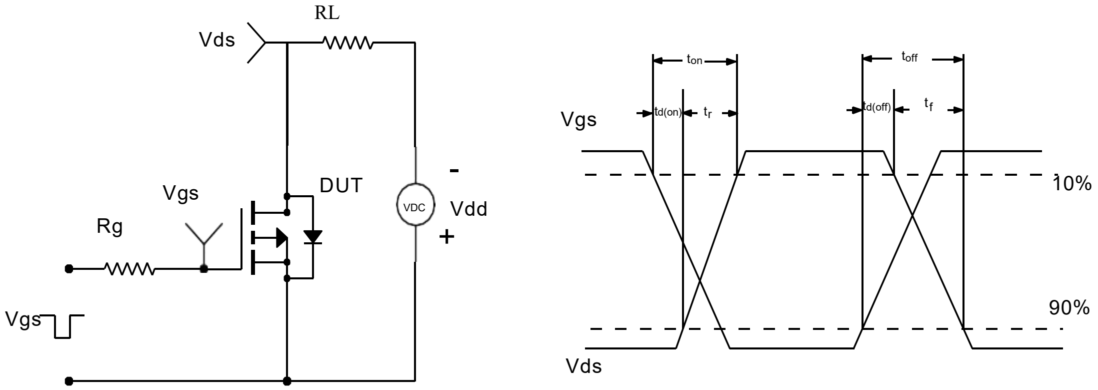
Figure 11. Transient Thermal Response Curve

P- Channel

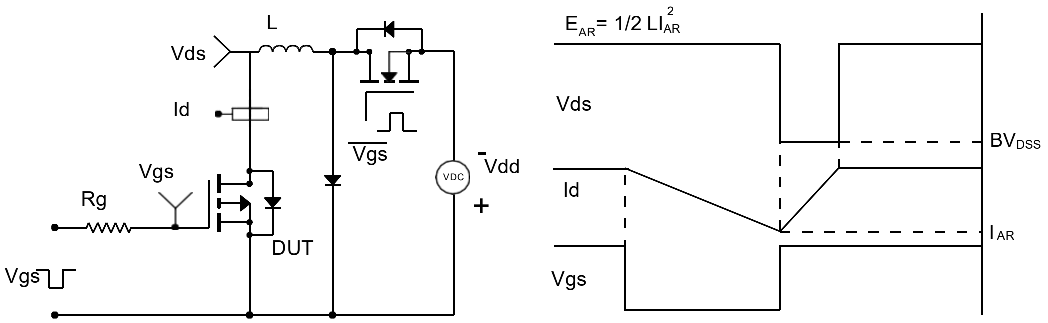
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

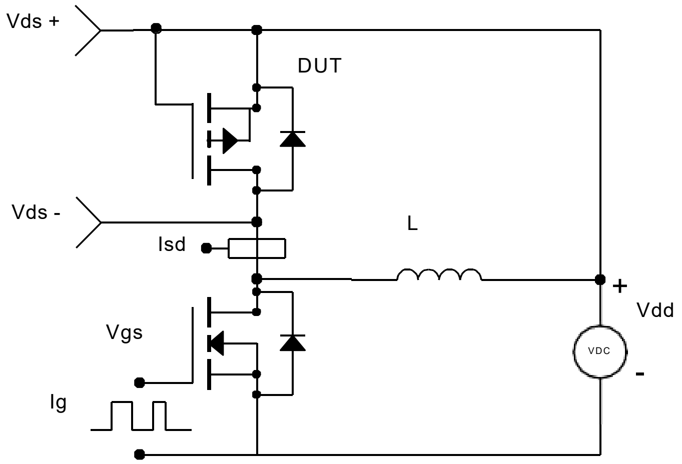


Unclamped Inductive Switching Test Circuit & Waveforms

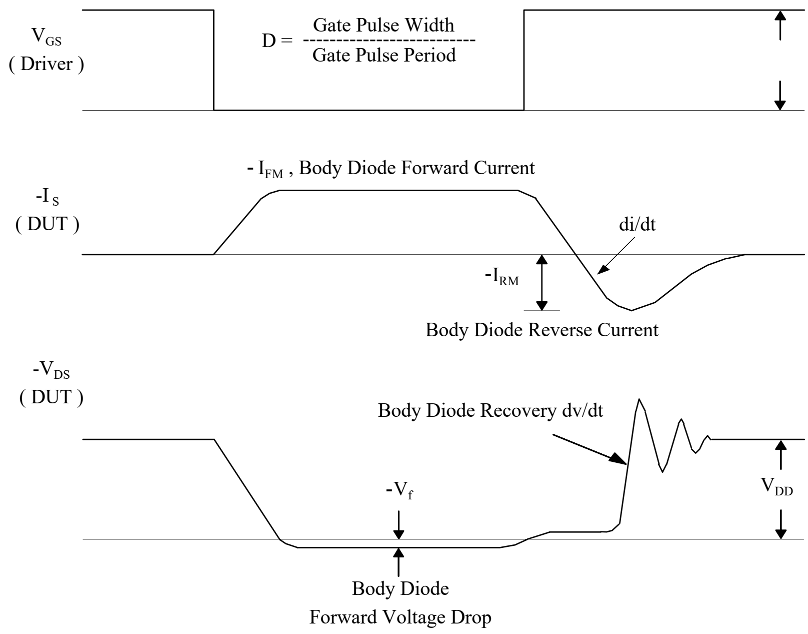


P- Channel

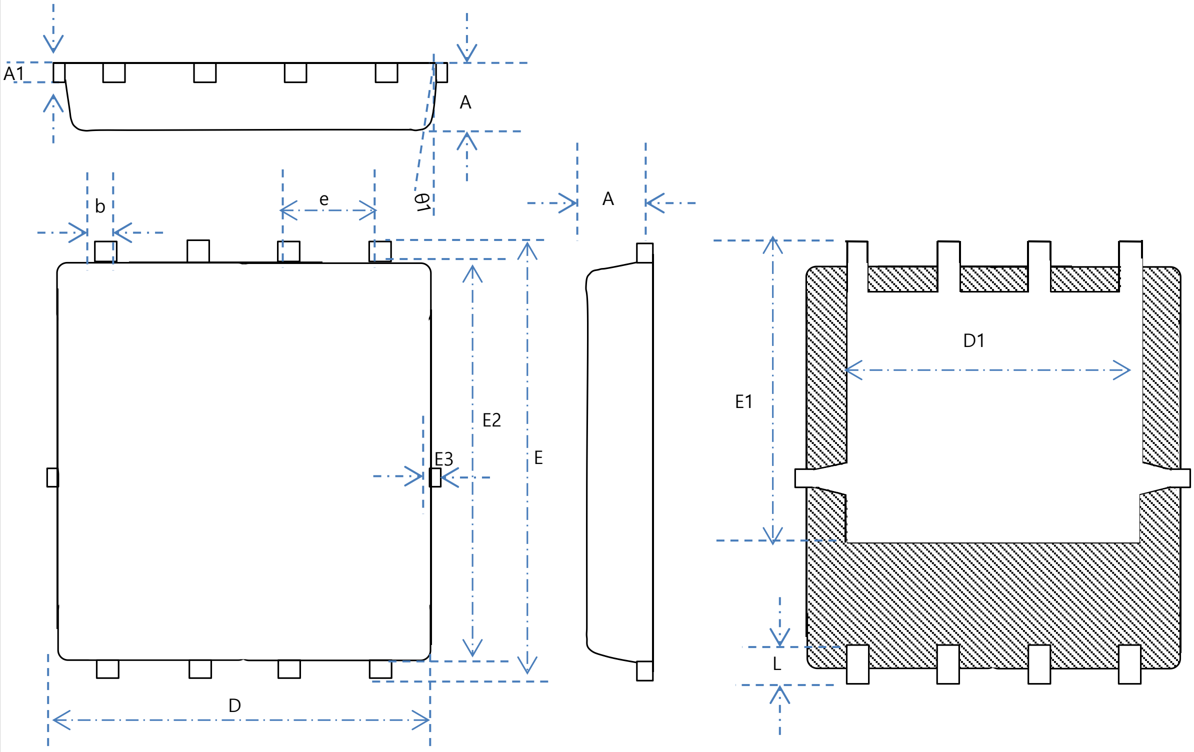
Peak Diode Recovery dv/dt Test Circuit & Waveforms



- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



DFN 3*3 OUTLINE



SYMBOL	Mechanical Dimensions/mm			SYMBOL	Mechanical Dimensions/mm		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.725	0.775	0.825	D	3.05	3.15	3.25
A1	0.152 REF			e	0.65 TYPE		
b	0.27	0.32	0.37	D1	2.25	2.45	2.65
E	3.25	3.35	3.45	L	0.28	0.38	0.48
E1	1.63	1.73	1.83				
E2	3.0	3.1	3.2	θ1	8^0	10^0	12^0
E3	-	-	0.10				

NAME	DFN 3*3 OUTLINE	UNIT	mm	DESIGNED	Shawn	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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