

SLV702T

20V N-Channel MOSFET

General Description

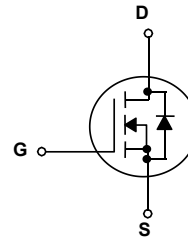
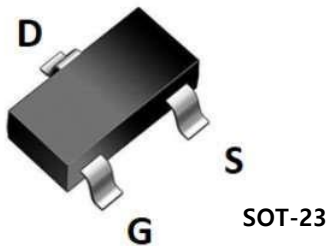
This Power MOSFET is produced using Msemitek's advanced TRENCH technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

- PWM Application
- Load Switch
- Power Management

Features

- N-Channel: 20V 9A
 $R_{DS(on)Typ} = 9.7m\Omega @ V_{GS} = 4.5V$
 $R_{DS(on)Typ} = 13.4m\Omega @ V_{GS} = 2.5V$
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLV702T	Units
V_{DSS}	Drain-Source Voltage	20	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	9	A
		5.8	A
I_{DM}	Drain Current - Pulsed (Note 1)	36	A
V_{GSS}	Gate-Source Voltage	± 20	V
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	1.25	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	$^\circ\text{C/W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLV702T	702T	SOT-23	Tape & Reel	3000	180000

Electrical Characteristics

 $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 10\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -10\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	0.67	1.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$	--	9.7	11	m Ω
		$V_{GS} = 2.5\text{ V}, I_D = 2\text{ A}$	-	13.4	15	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	993	-	pF
C_{oss}	Output Capacitance		--	200	-	pF
C_{rss}	Reverse Transfer Capacitance		--	190	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 5\text{ A},$ $R_G = 3\ \Omega$	--	6	--	ns
t_r	Turn-On Rise Time		--	13	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	67	--	ns
t_f	Turn-Off Fall Time		--	18	--	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 4.5\text{ V}$	--	14	--	nC
Q_{gs}	Gate-Source Charge		--	1.6	--	nC
Q_{gd}	Gate-Drain Charge		--	4.3	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	36	A
V_{SD}	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = 1\text{ A}, T_J = 25^\circ\text{C}$	--	--	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Device mounted on FR-4 PCB, 1inch x 0.85inch x 0.062 inch
3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 0.5%

N- Channel Typical Characteristics

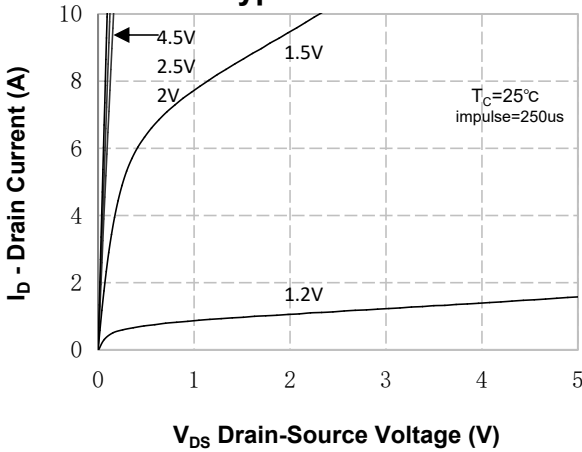


Figure 1. On-Region Characteristics

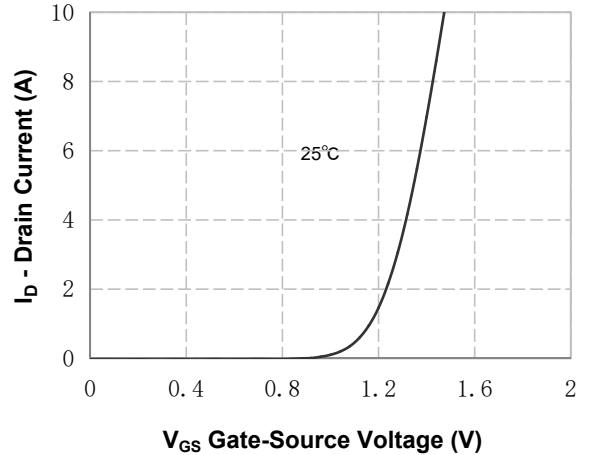


Figure 2. Transfer Characteristics

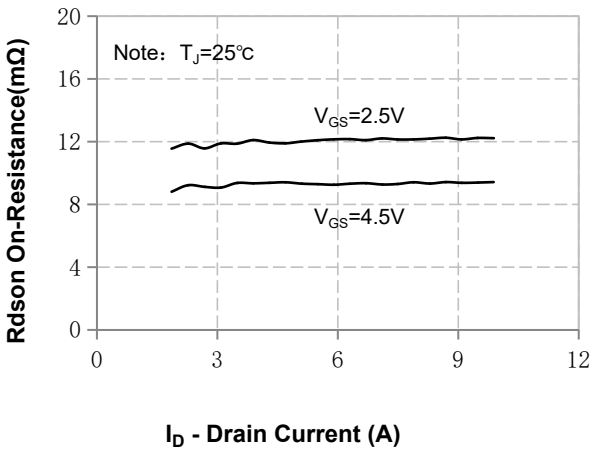


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

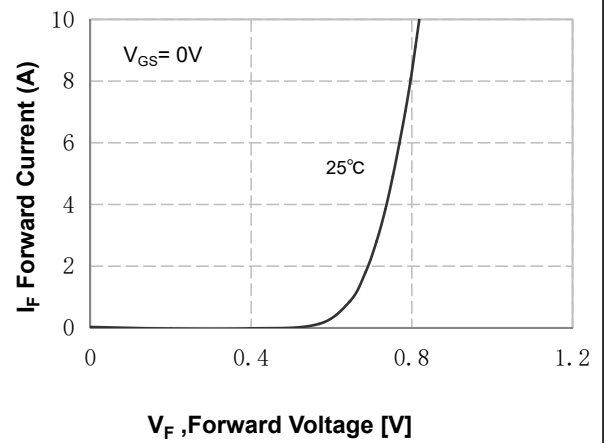


Figure 4. Body Diode Forward Voltage Variation vs Source Current

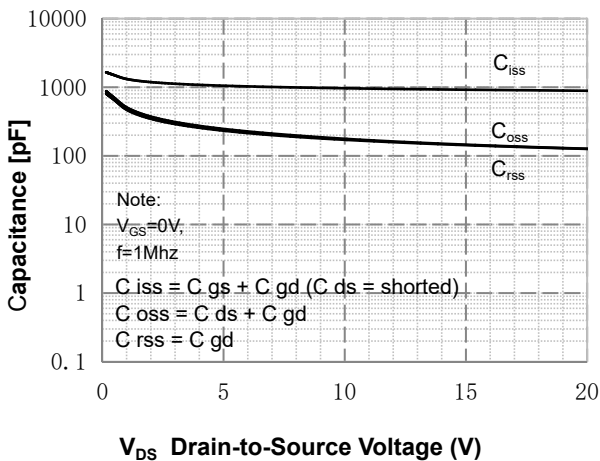


Figure 5. Capacitance Characteristics

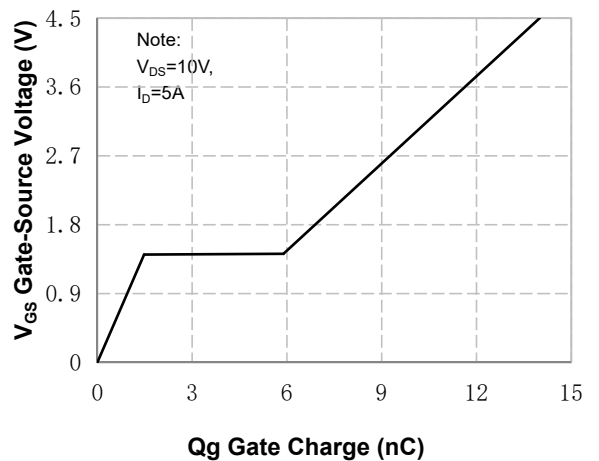


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

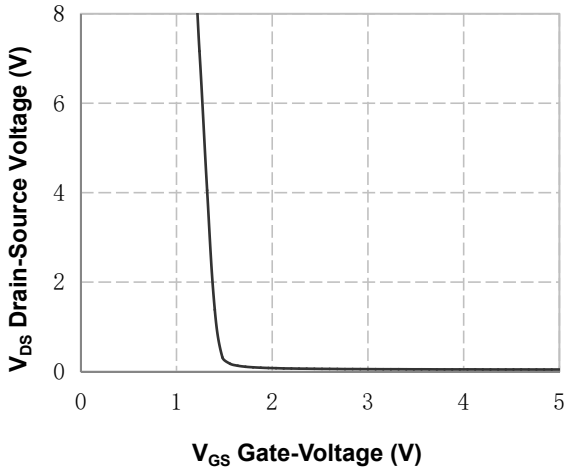


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

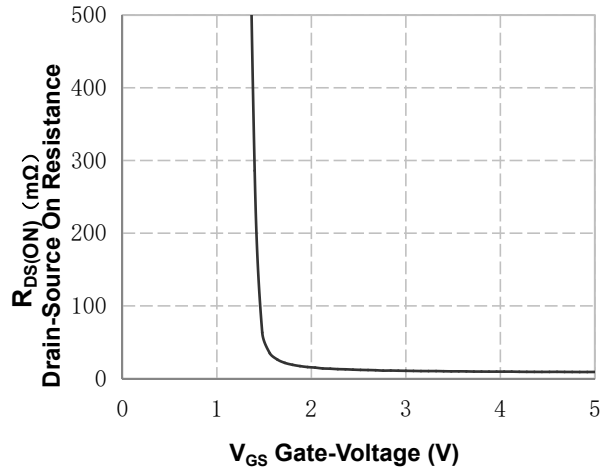


Figure 8. On-Resistance vs Gate Voltage

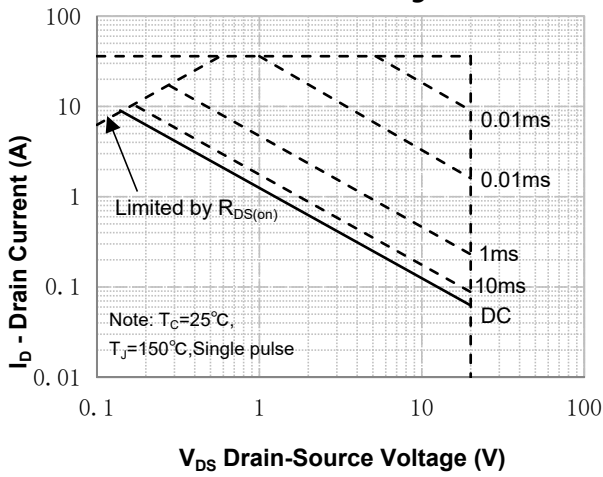


Figure 9. Maximum Safe Operating Area

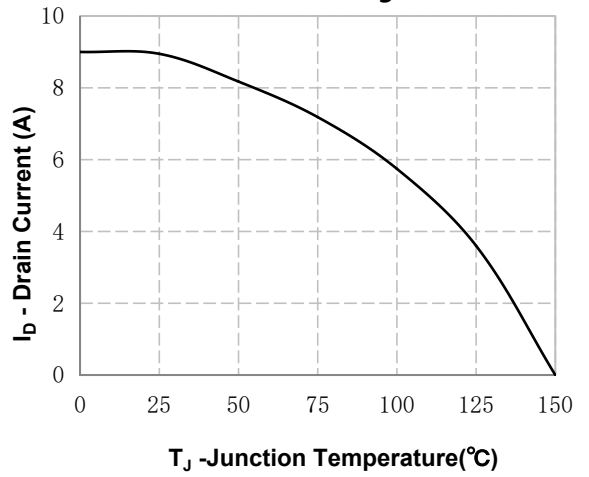


Figure 10. Maximum Continuous Drain Current vs Temperature

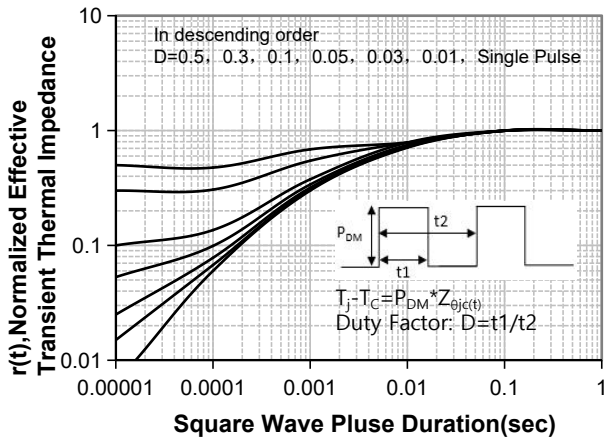
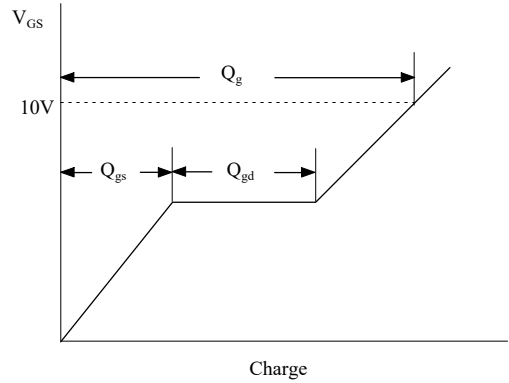
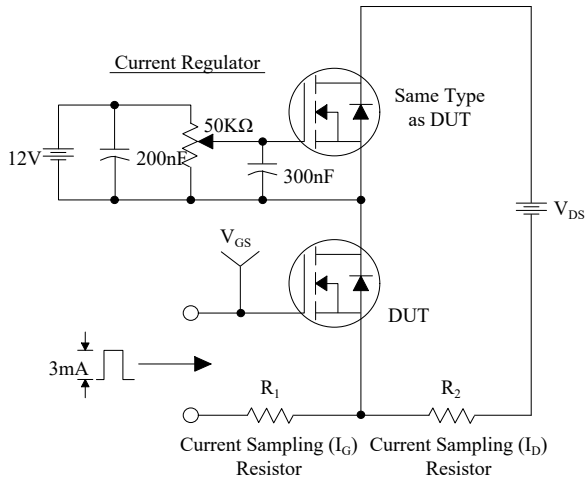
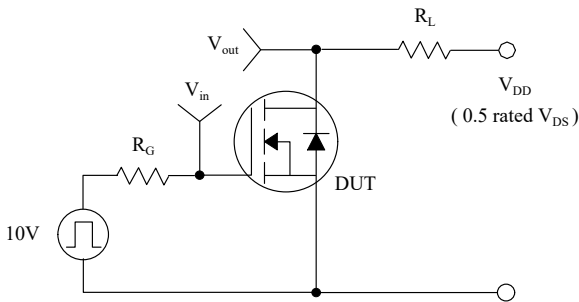


Figure 11. Transient Thermal Response Curve

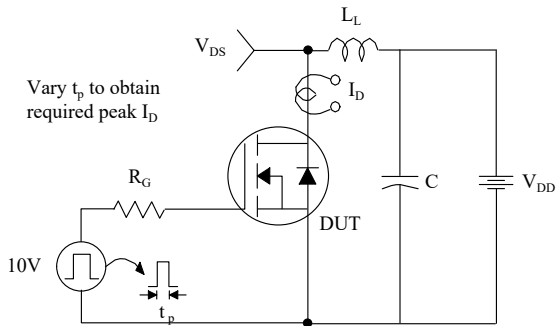
Gate Charge Test Circuit & Waveform



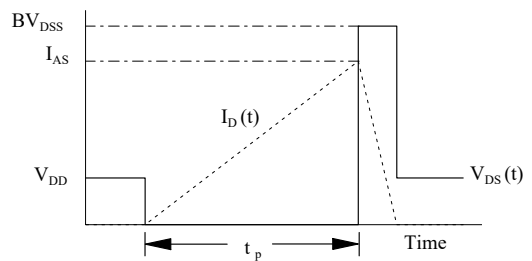
Resistive Switching Test Circuit & Waveforms



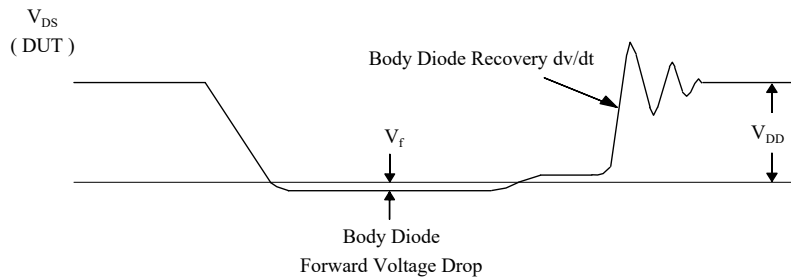
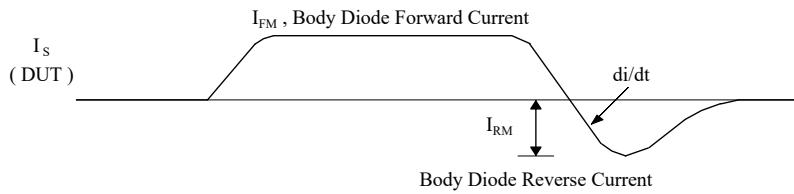
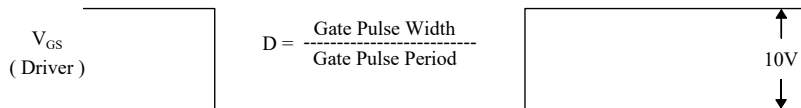
Unclamped Inductive Switching Test Circuit & Waveforms



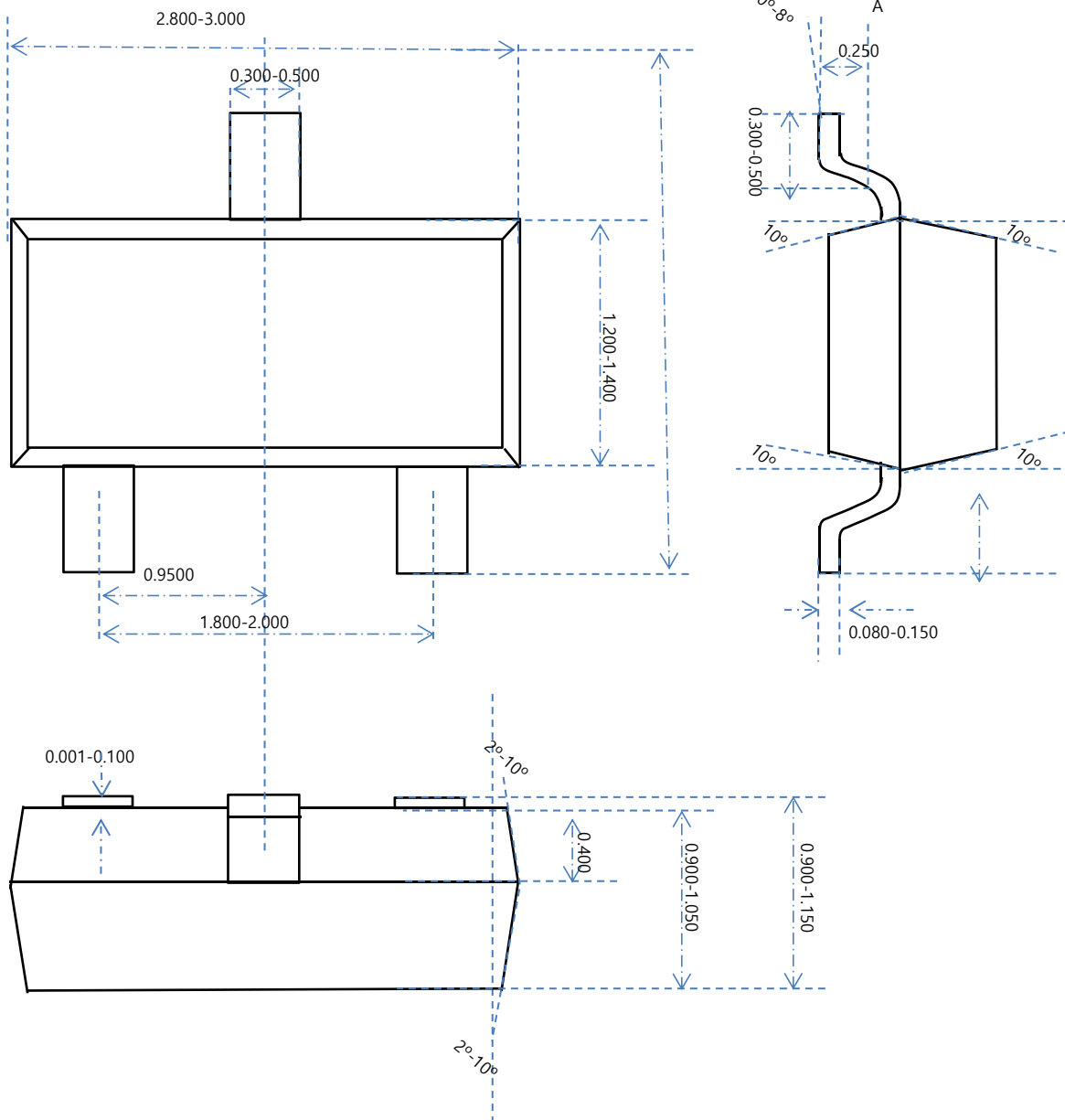
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms



SOT-23 OUTLINE



NOTE:

- 1.The plastic package is not marked as smooth surfaceRa=0.1; Subglossy surfaceRa=0.8
- 2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

NAME	SOT-23 OUTLINE	UNIT	mm	DESIGNED	Shawn	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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