美浦森半导体
Msemitek

RoHS
LEAD FREE

SLV123TK
# 100V N -Channel MOSFET

General Description
This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application
☑ PWM Application
☑ Load Switch
☑ Power Management

Features
- N-Channel:100V 0.17A
  $R_{DS(on)Typ}$= 4Ω@V_{GS} = 10V
  $R_{DS(on)Typ}$= 6 Ω@V_{GS} = 4.5V
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

SOT-23
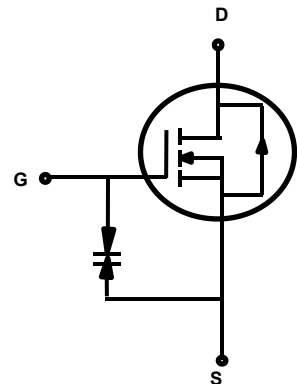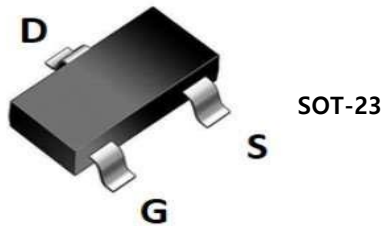
Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		SLV123TK	Units
V_{DSS}	Drain-Source Voltage		100	V
I_D	Drain Current — Continuous (T_C = 25°C)		0.17	A
	— Continuous (T_C = 100°C)		0.11	A
I_{DM}	Drain Current — Pulsed	(Note 1)	0.68	A
V_{GSS}	Gate-Source Voltage		±20	V
P_D	Power Dissipation (T_C = 25°C)		35	W
$R_{θJC}$	Thermal Resistance, Junction to Case		357	°C/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

* Drain current limited by maximum junction temperature.

Electrical Characteristics
T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =100 V, V_{GS} = 0 V	--	--	1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	10	uA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-10	uA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	1.5	2	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} =10 V, I_D = 0.5A	--	4	6	Ω
		V_{GS} =4.5V, I_D = 0.5A	--	6	9	Ω

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	60	-	pF
C_{oss}	Output Capacitance		--	15	-	pF
C_{rss}	Reverse Transfer Capacitance		--	6	-	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=10V, V_{DS}=30 V, R_G = 50 Ω ,I_D=0.1A	--	8	--	ns
t_r	Turn-On Rise Time		--	8	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	13	--	ns
t_f	Turn-Off Fall Time		--	6	--	ns
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D =0.2A, V_{GS} = 10V	--	2	--	nC
Q_{gs}	Gate-Source Charge		--	0.25	--	nC
Q_{gd}	Gate-Drain Charge		--	0.4	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	0.17	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	0.68	A
V_{SD}	Drain to Source Diode Forward Voltage,V GS = 0V, I SD =0.2A,T J = 25°C	--	--	1.2	V

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%
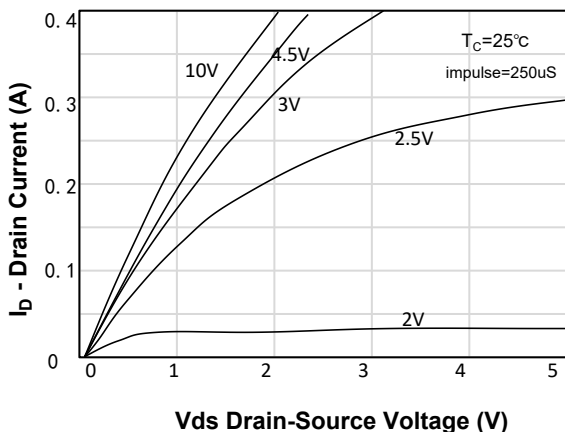
N- Channel Typical Characteristics

Vds Drain-Source Voltage (V)

Figure 1. On-Region Characteristics

Vgs Gate-Source Voltage (V)
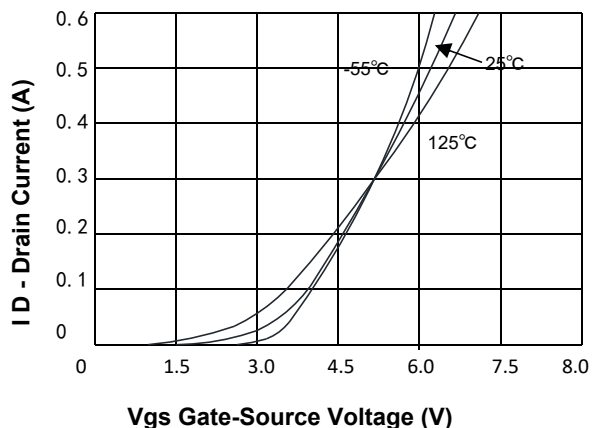
Figure 2. Transfer Characteristics
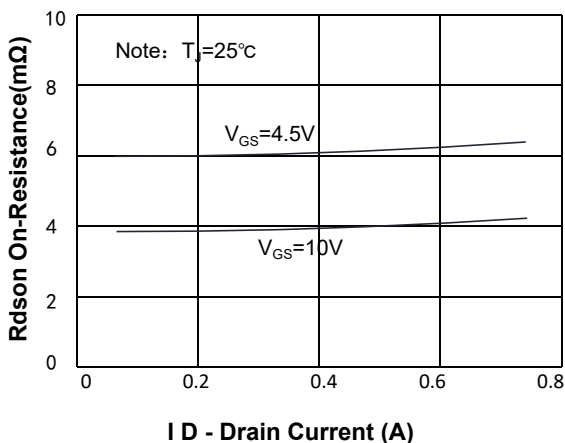
I D - Drain Current (A)

Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

V F ,Forward Voltage [V]
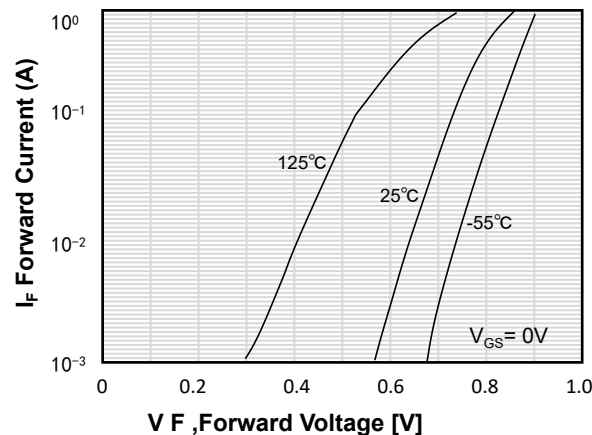
Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

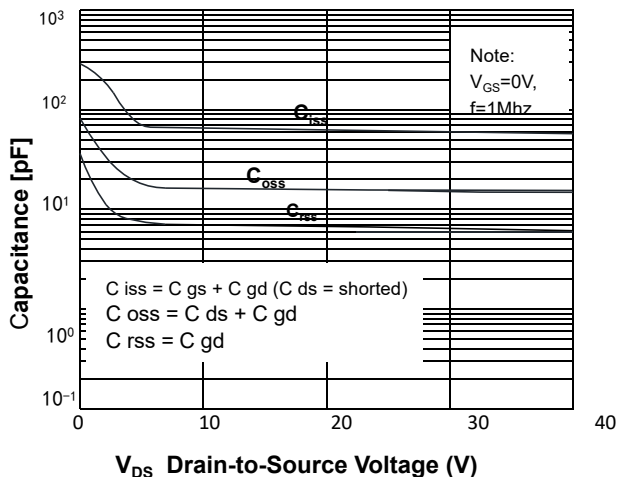V_{DS} Drain-to-Source Voltage (V)

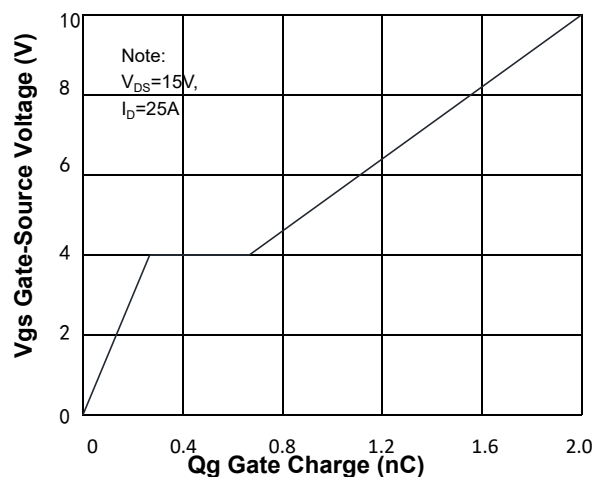**Figure 5. Capacitance Characteristics**

Qg Gate Charge (nC)

Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)
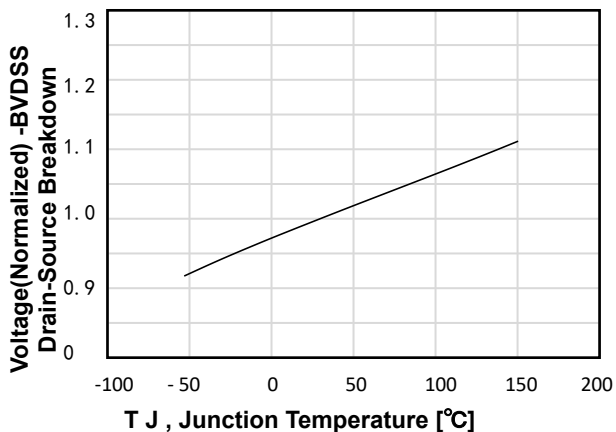
Figure 7. Breakdown Voltage Variation vs Temperature

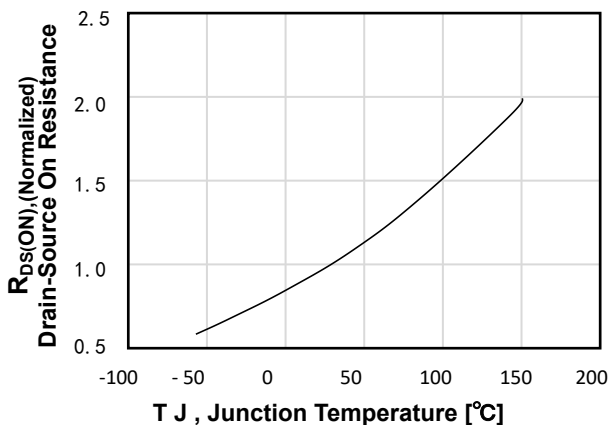(Plot: Voltage(Normalized) -BVDSS Drain-Source Breakdown vs T J , Junction Temperature [°C])

Figure 8. On-Resistance Variation vs Temperature

(Plot: $R_{DS(ON)}$ (Normalized) Drain-Source On Resistance vs T J , Junction Temperature [°C])
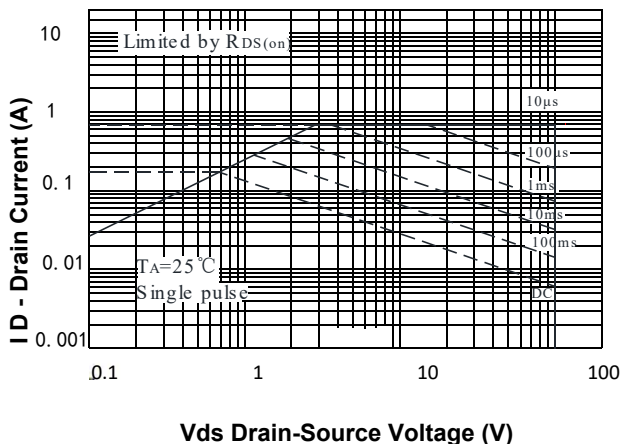
Figure 9. Maximum Safe Operating Area

Limited by $R_{DS(on)}$

10μs
100μs
1ms
10ms
100ms
DC

$T_A=25°C$
Single pulse
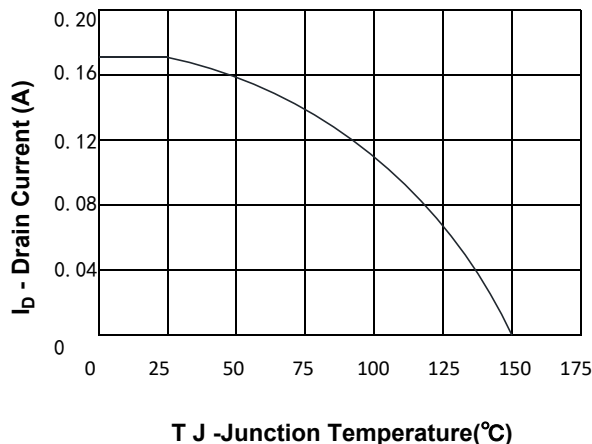
(Plot: I D - Drain Current (A) vs Vds Drain-Source Voltage (V))

Figure 10. Maximum Continuous Drain Current vs Temperature

(Plot: I_D - Drain Current (A) vs T J -Junction Temperature(°C))
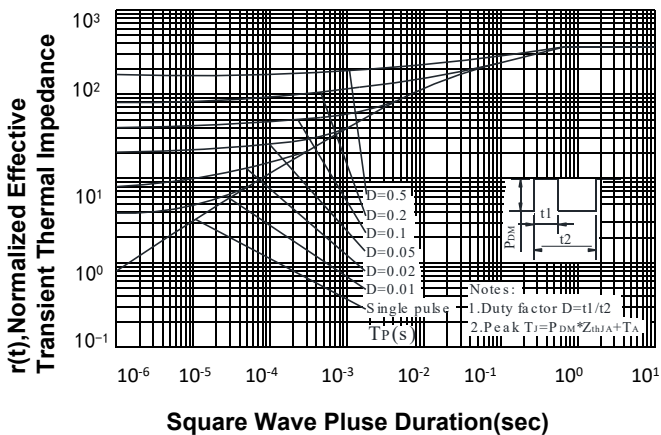
Figure 11. Transient Thermal Response Curve

D=0.5
D=0.2
D=0.1
D=0.05
D=0.02
D=0.01
Single pulse
$T_P(s)$

Notes:
1.Duty factor D=t1/t2
2.Peak $T_J=P_{DM}*Z_{thJA}+T_A$

(Plot: r(t),Normalized Effective Transient Thermal Impedance vs Square Wave Pluse Duration(sec))
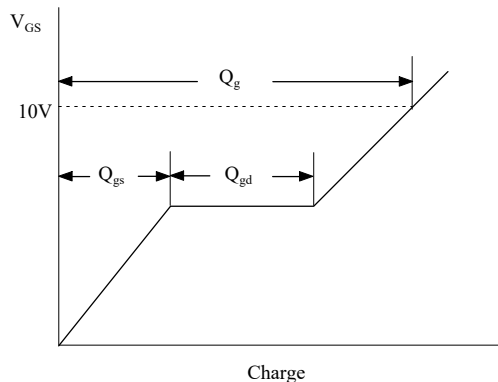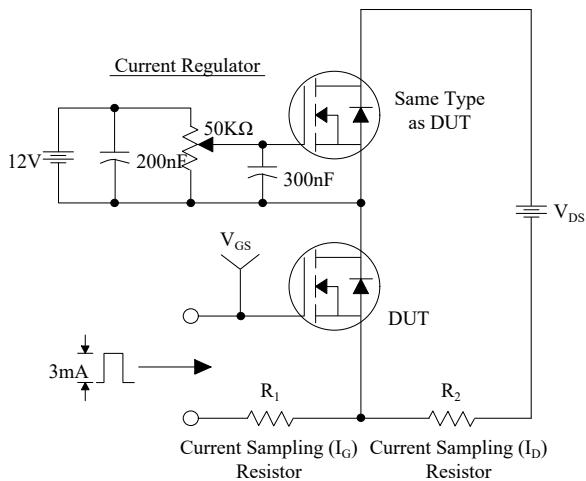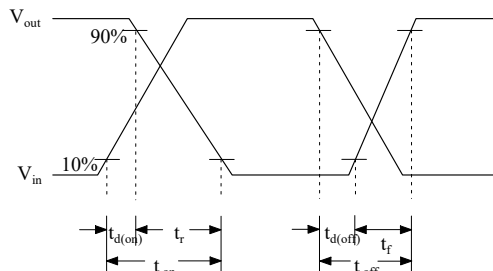
Gate Charge Test Circuit & Waveform

Current Regulator

12V 200nF 50KΩ 300nF

Same Type
as DUT

V_{DS}

V_{GS}

DUT

3mA

R_1 R_2

Current Sampling (I_G)   Current Sampling (I_D)
Resistor   Resistor

V_{GS}

10V

Q_g

Q_{gs} Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

V_{out} R_L

V_{in}

V_{DD}
(0.5 rated V_{DS})

R_G

DUT

10V

V_{out}

90%

V_{in} 10%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
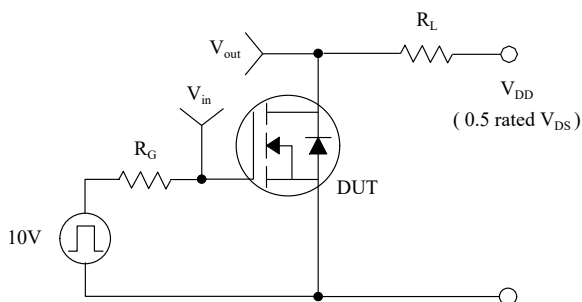
Unclamped Inductive Switching Test Circuit & Waveforms

L_L

V_{DS}

I_D

Vary t_p to obtain
required peak I_D

R_G

DUT

C V_{DD}

10V

t_p

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD}

$V_{DS}(t)$

t_p Time
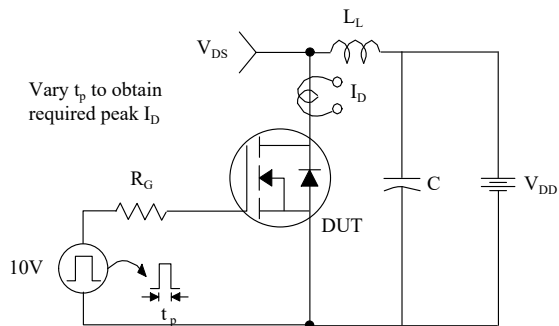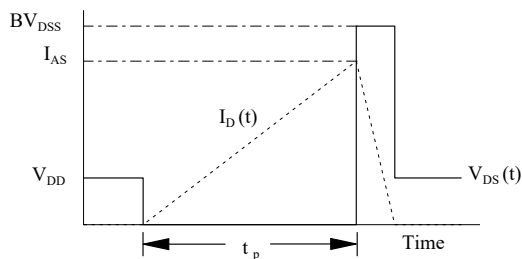
Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

+

--

I_S

L

V_{GS}

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R$_G$

• I$_{SD}$ controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_S
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_f

V_{DD}

Body Diode
Forward Voltage Drop

SOT-23 OUTLINE

2.800-3.000

0.300-0.500

1.200-1.400

0.9500

1.800-2.000

0°-8°

A

0.250

0.300-0.500

10° 10°

10° 10°

0.080-0.150

0.001-0.100

2°-10°

0.400

0.900-1.050

0.900-1.150

2°-10°

NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;   Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

NAME	SOT-23 OUTLINE	UNIT	mm	DESIGNED	Shawn	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

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