美浦森半导体
M s e m i t e k

RoHS
LEAD FREE

SLP18N20T/SLF18N20T
200V N -Channel MOSFET

General Description

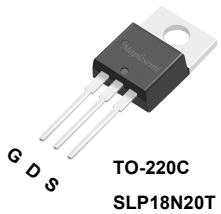
This Power MOSFET is produced using Msemitek's advanced TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

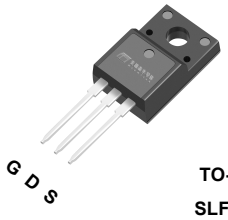
☑PWM Application
☑Load Switch
☑Power Management

Features

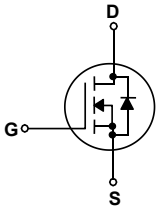
- N-Channel:200V 18A
  $R_{DS(on)Typ}$= 120mΩ@V_{GS} = 10 V
- Very Low On-resistance $R_{DS(ON)}$
- Low Crss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220C
SLP18N20T



TO-220F
SLF18N20T



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLP18N20T/SLF18N20T	Units
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current - Continuous (T_C = 25℃)	18	A
	Drain Current - Continuous (T_C = 100℃)	11.3	A
I_{DM}	Drain Current - Pulsed (Note 1)	72	A
V_{GSS}	Gate-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	500	mJ
P_D	Power Dissipation (T_C = 25℃)	44	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.85	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to ambient	62.5	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLP18N20T	SLP18N20T	T0-220	Tube	1000	5000
SLF18N20T	SLF18N20T	TO-220F	Tube	1000	5000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	200	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =200 V, V_{GS} = 0 V	--	--	1.0	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D =8.4A	--	120	180	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1180	-	pF
C_{oss}	Output Capacitance		--	155	-	pF
C_{rss}	Reverse Transfer Capacitance		--	70	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= 10 V, V_{DS}=100V, R_L = 10 Ω ,,I_D=18A (Note 3)	--	19	--	ns
t_r	Turn-On Rise Time		--	33	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	--	ns
t_f	Turn-Off Fall Time		--	8	--	ns
Q_g	Total Gate Charge	V_{DS} = 100 V, I_D =18A, V_{GS} = 10V (Note 3)	--	30	--	nC
Q_{gs}	Gate-Source Charge		--	6.5	--	nC
Q_{gd}	Gate-Drain Charge		--	7.3	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	18	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	72	A
VF_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =20A,T J = 25℃		--	-	1.5	V
T_{rr}	Reverse recovery time,I_F =18A D_I /dt=100A/μs			190		ns
Q_{rr}	Reverse recovery charge,I_F =18A D_{IF} /dt=100A/μs			920		nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T J =25℃, V_{DD} =30V, V_G =10V, L=10mH,
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

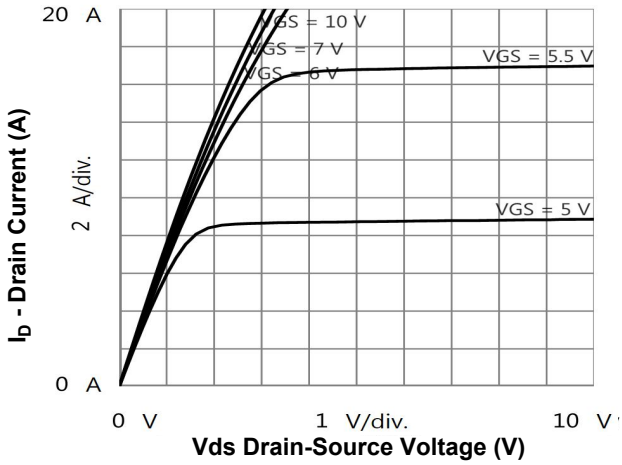


Figure 1. On-Region Characteristics

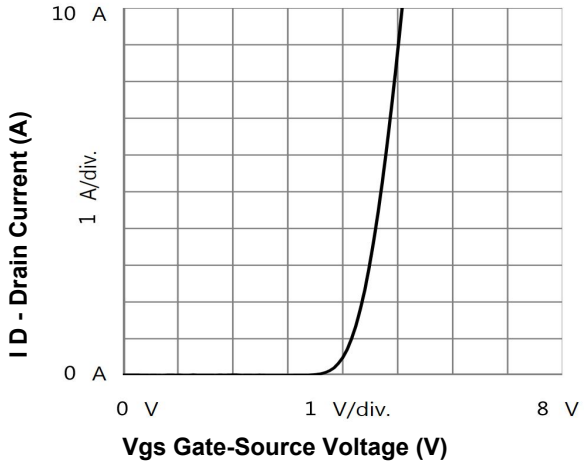


Figure 2. Transfer Characteristics

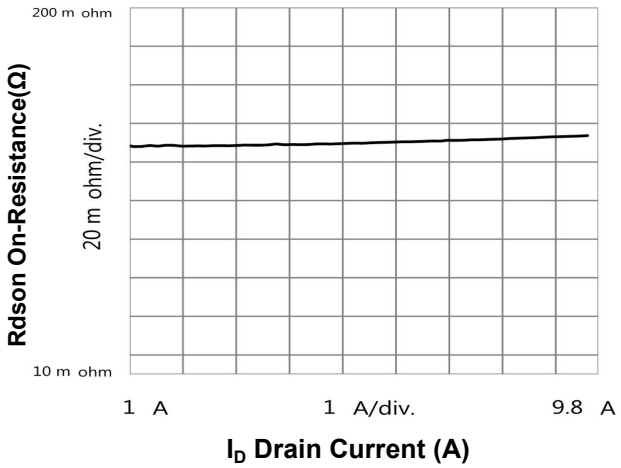


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

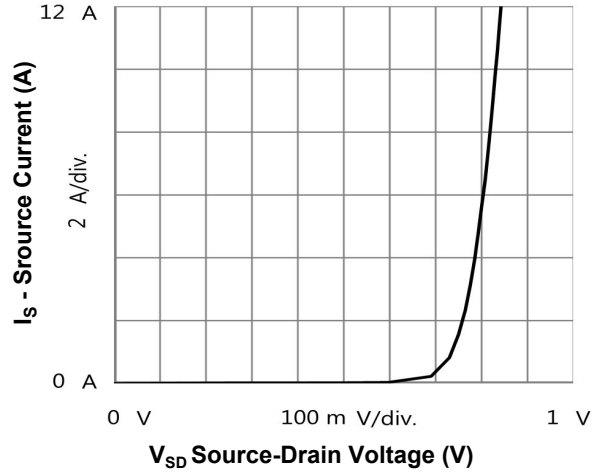


Figure 4. Source Current vs Source-Drain Voltage

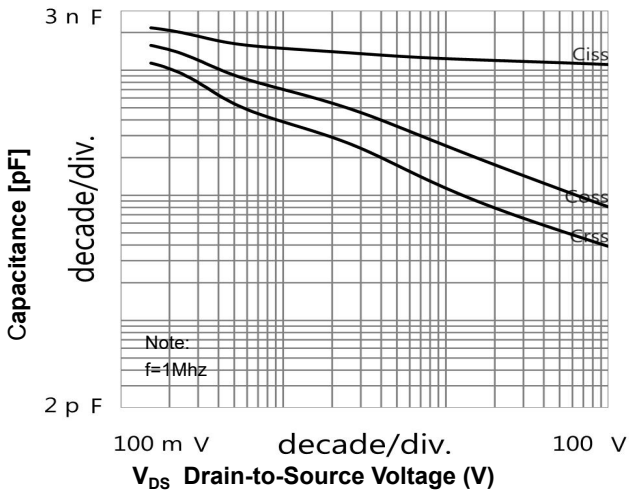


Figure 5.1 Capacitance Characteristics

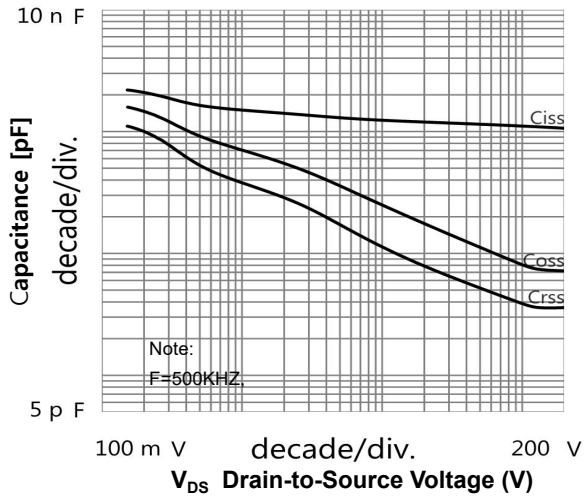


Figure 5.2 Capacitance Characteristics

N- Channel Typical Characteristics (Continued)

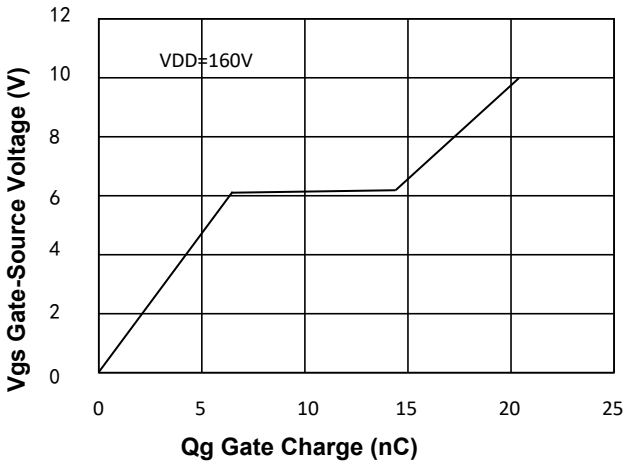


Figure 6. Gate Charge Characteristics

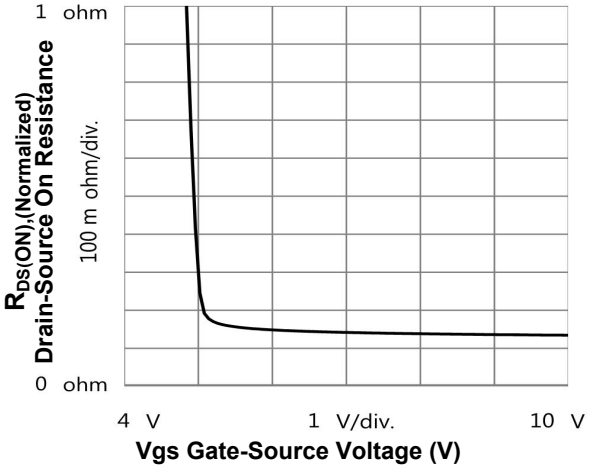


Figure 7. On-Resistance Variation vs Gate-Source Voltage

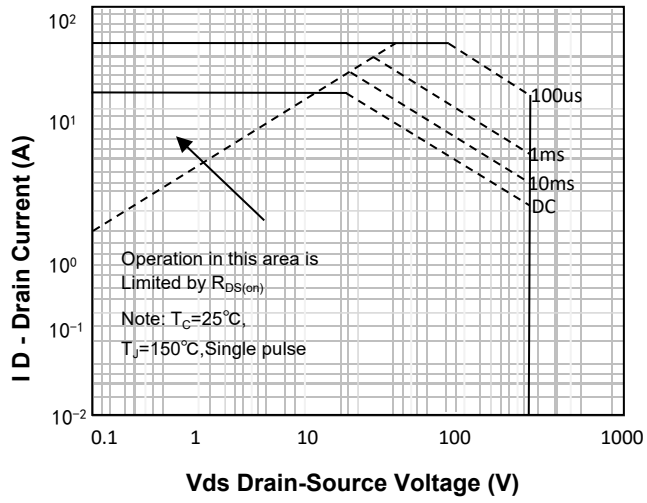


Figure 8. Maximum Safe Operating Area

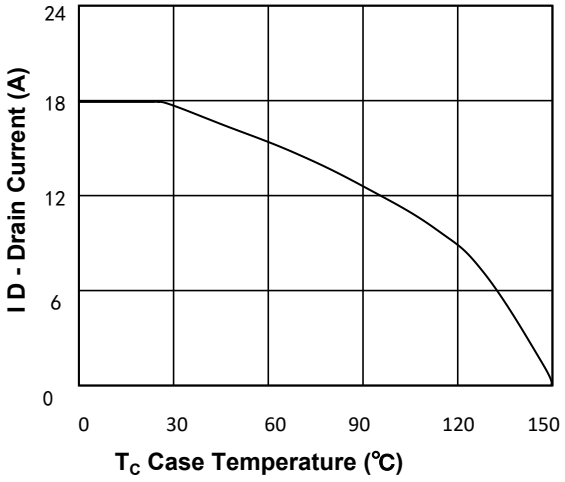


Figure 9. aximum Drain Current vs Case Temperature

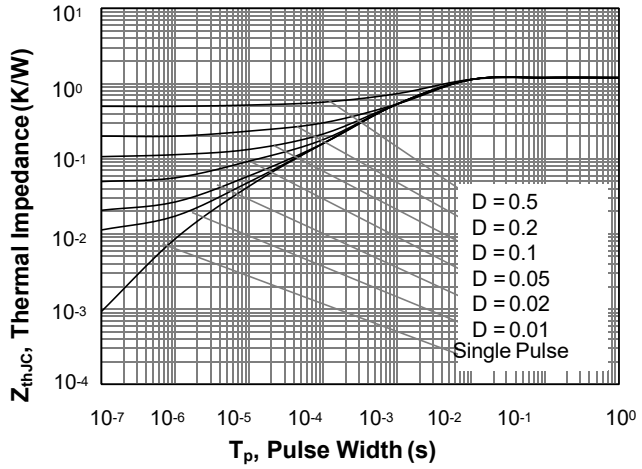
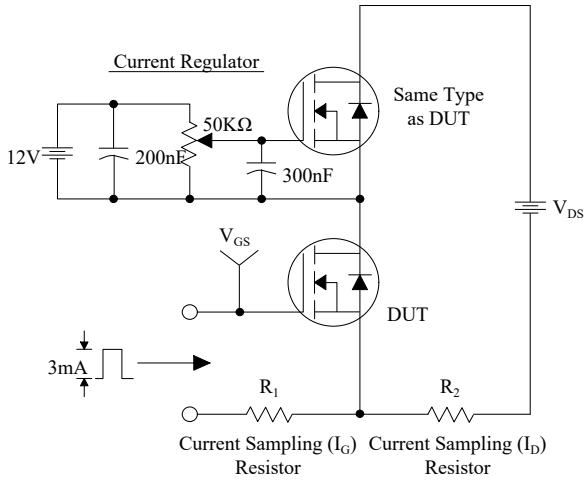
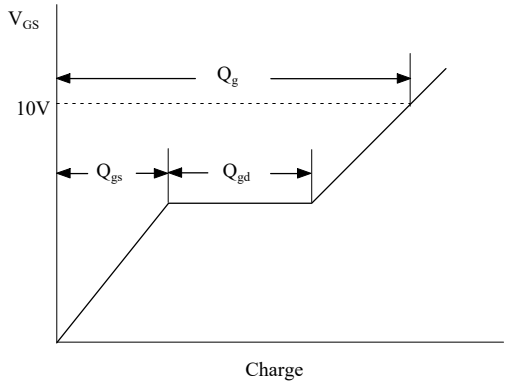


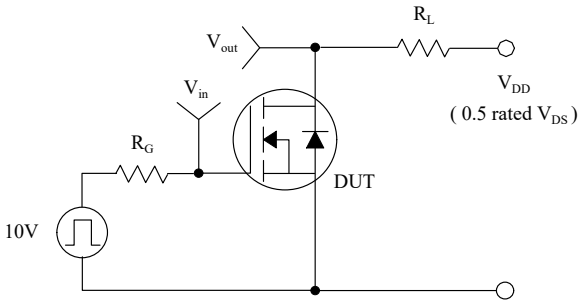
Figure 10. Transient Thermal Response Curve

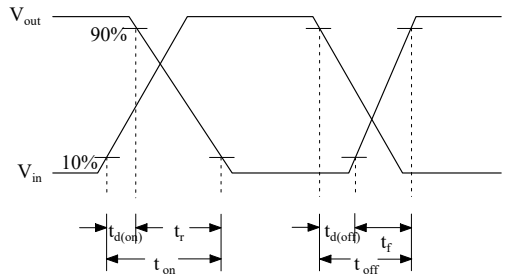
Gate Charge Test Circuit & Waveform



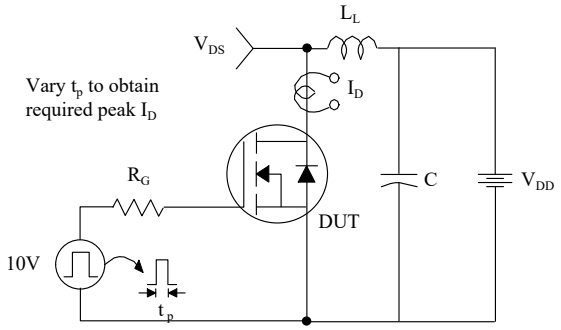


Resistive Switching Test Circuit & Waveforms

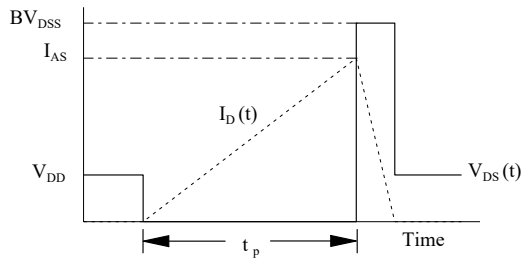




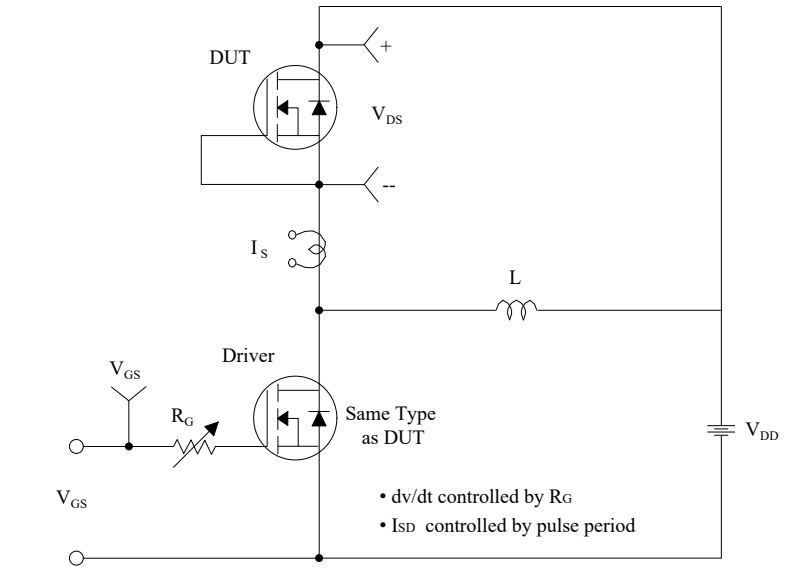
Unclamped Inductive Switching Test Circuit & Waveforms

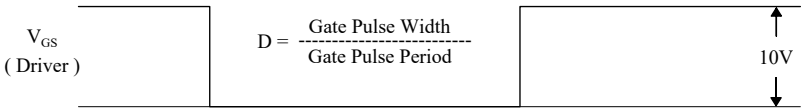


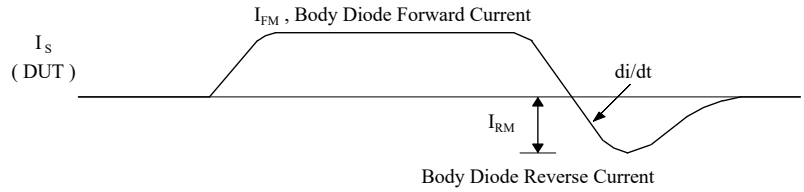
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

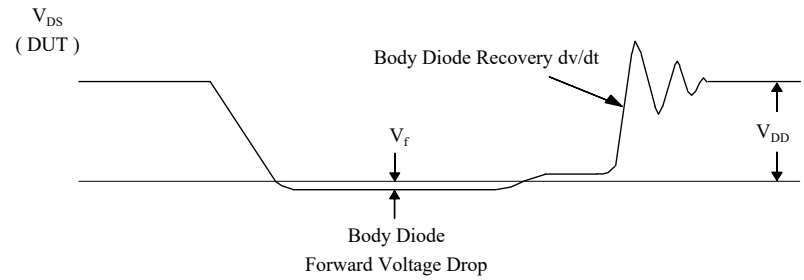


Peak Diode Recovery dv/dt Test Circuit & Waveforms

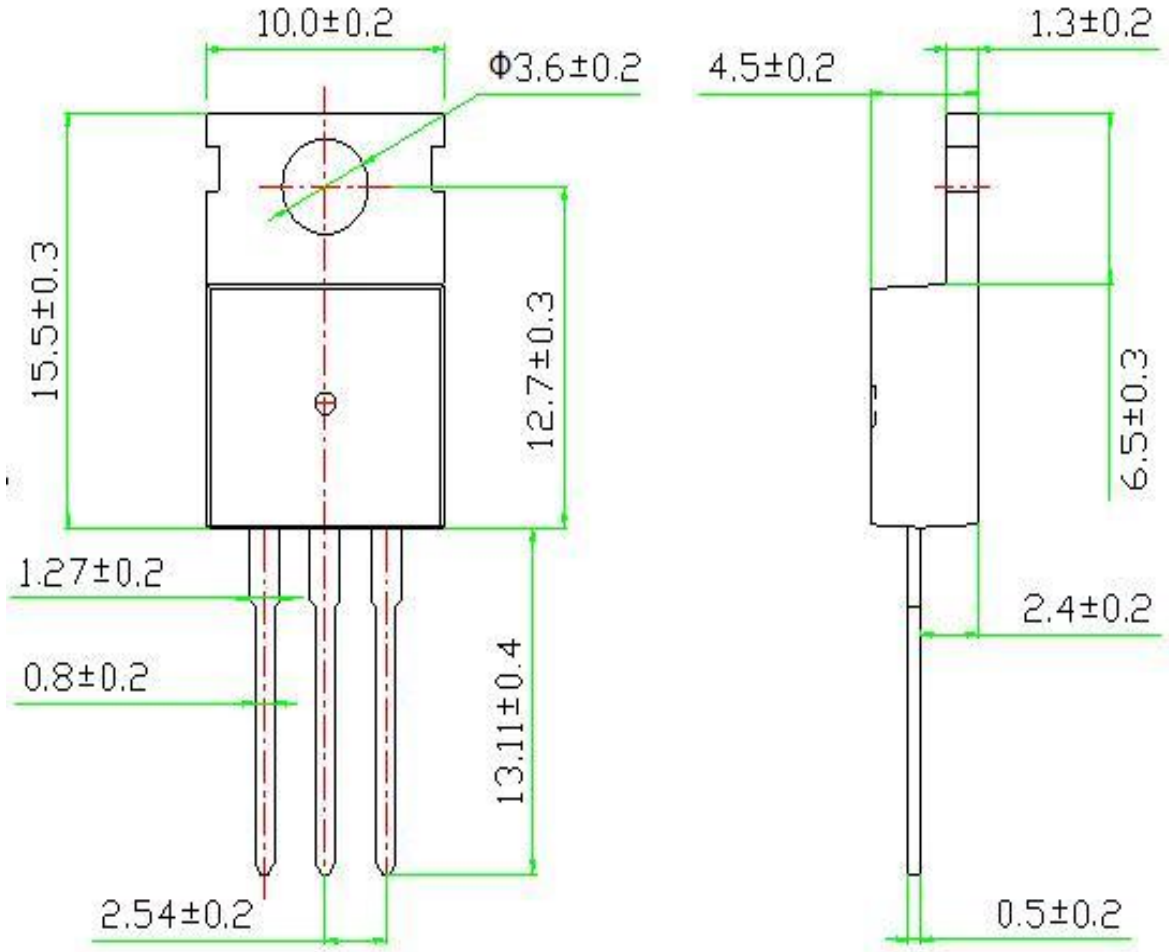






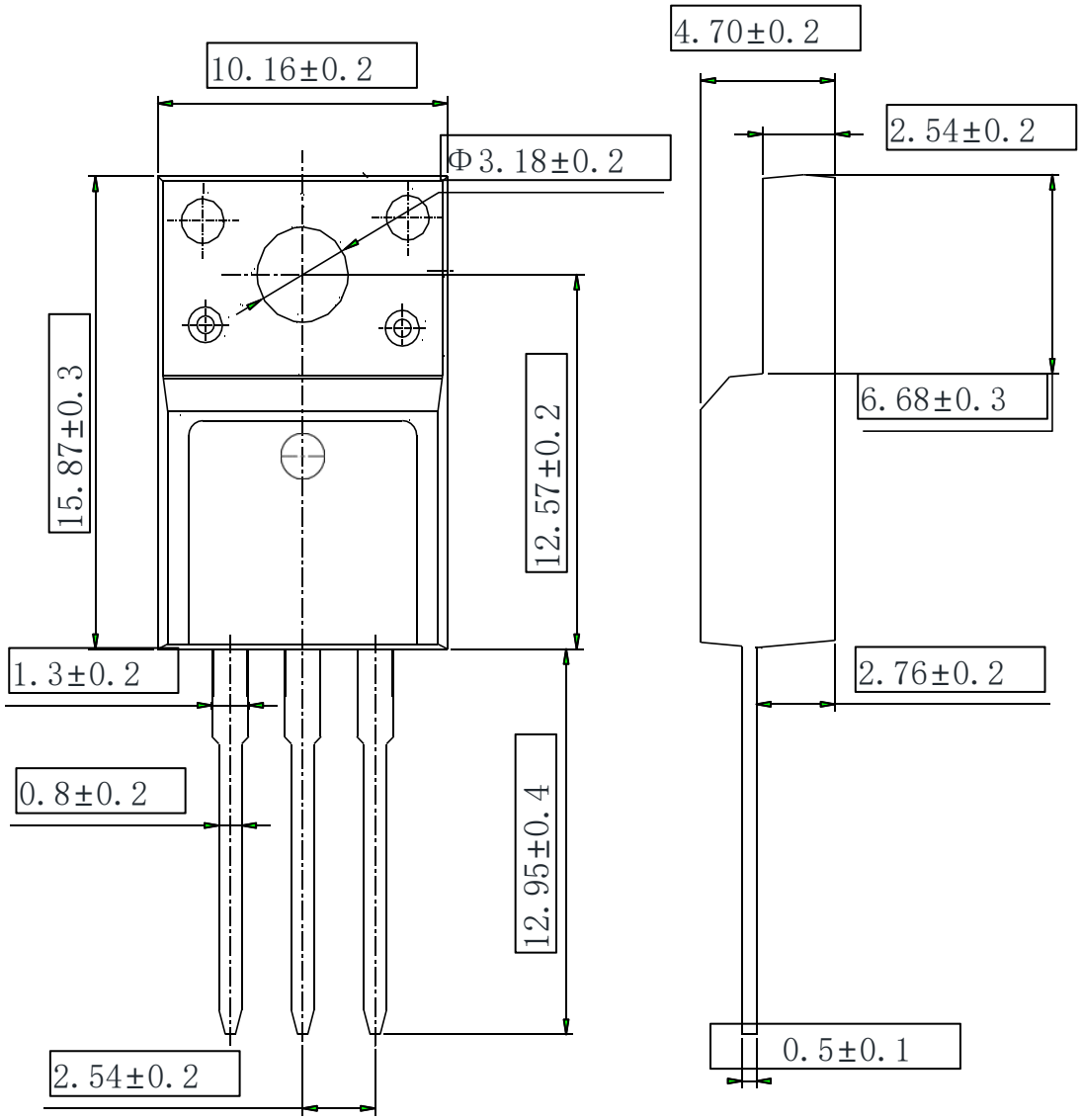


TO-220C OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

TO-220F OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.15,Unmarked filletRmax=0.25

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