Maplesemi

LEAD FREE RoHS

SLD20N15T
150V N -Channel MOSFET

General Description

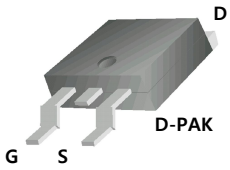
This Power MOSFET is produced using Maple semi's advanced planar stripe TRENCH technology.
This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

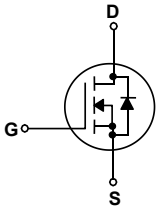
Features

- N-Channel:150V 20A
  $R_{DS(on)Typ}$= 70mΩ@V_{GS} = 10 V
  $R_{DS(on)Typ}$= 84mΩ@V_{GS} = 7 V
- Very Low On-resistance RDS(ON)
- LowCrss
- Extremely low switching loss
- Excellent stability and uniformity
- Split gate trench MOSFET technology

Application

- Synchronous Rectification in DC/DC and AC/DC Converters
- Industrial and Motor Drive applications





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLD20N15T	Units
V_{DSS}	Drain-Source Voltage	150	V
I_D	Drain Current - Continuous (T_C = 25℃)	20	A
	Drain Current - Continuous (T_C = 100℃)	13	A
I_{DM}	Drain Current - Pulsed (Note 1)	80	A
V_{GSS}	Gate-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy	181	mJ
P_D	Power Dissipation (T_C = 25℃)	89	W
	Power Dissipation (T_C = 100℃)	35.7	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to ambient	62.0	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD20N15T	SLD20N15T	D-Pak	Tape & Reel	2500	25000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	150	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =150 V, V_{GS} = 0 V	--	--	1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	3.5	-	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 10A	--	70	94	mΩ
		V_{GS} = 7 V, I_D = 10A	--	84	110	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1.0 MHz	--	898	-	pF
C_{oss}	Output Capacitance		--	60	-	pF
C_{rss}	Reverse Transfer Capacitance		--	30	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{GS}= 10 V, V_{DS}=30V, R_L = 3Ω ,I_D=1OA Tj=25℃	--	6.9	--	ns
t_r	Turn-On Rise Time		--	28	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	23	--	ns
t_f	Turn-Off Fall Time		--	19	--	ns
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D =10A, V_{GS} = 10V	--	20	--	nC
Q_{gs}	Gate-Source Charge		--	6.7	--	nC
Q_{gd}	Gate-Drain Charge		--	6.9	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	80	A
V_{SD}	Drain to Source Diode Forward Voltage,V GS = 0V, I SD =20A,T J = 25℃		--	-	1.4	V
T_{rr}	Reverse recovery time,I F =-20A DI F /dt=100A/μs			47		ns
Q_{rr}	Reverse recovery charge,I F =-20A DI F /dt=100A/μs			0.1		nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} =30V, R_G =25Ω, L=0.5mH, I_{AS} =13A
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

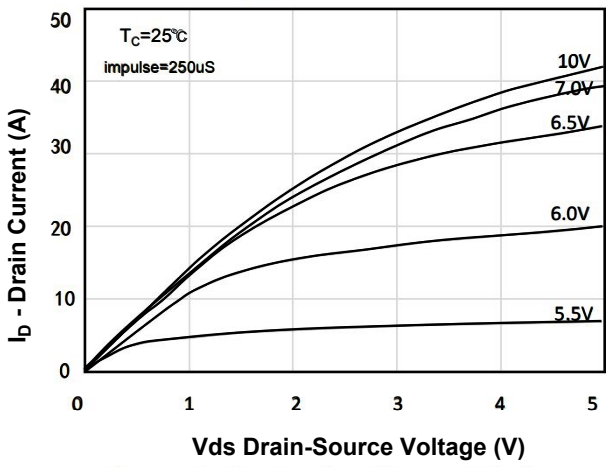


Figure 1. On-Region Characteristics

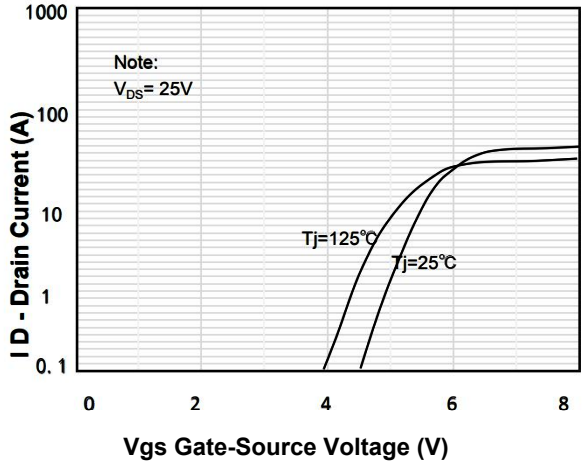


Figure 2. Transfer Characteristics

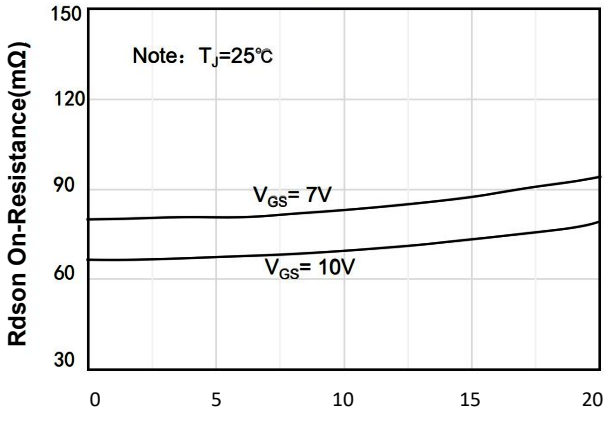


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

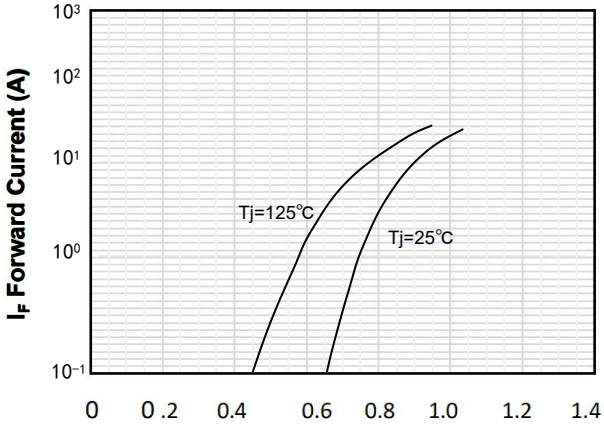


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

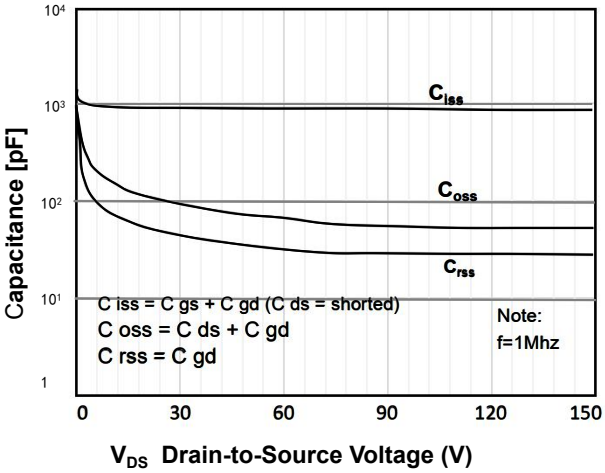


Figure 5. Capacitance Characteristics

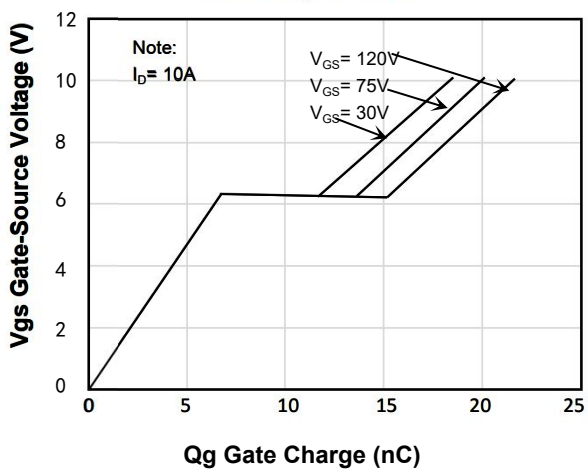


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

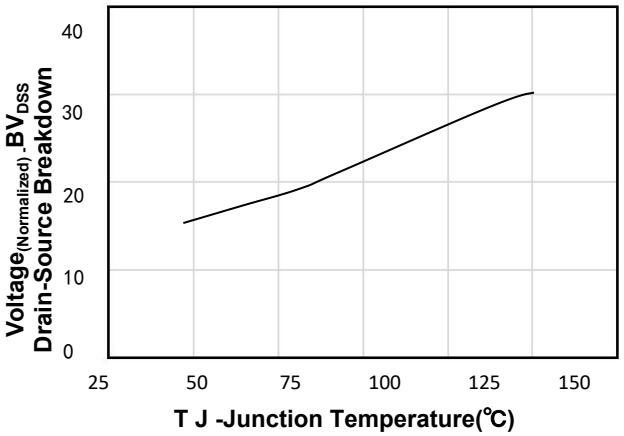


Figure 7. Breakdown Voltage Variation vs Case Temperature

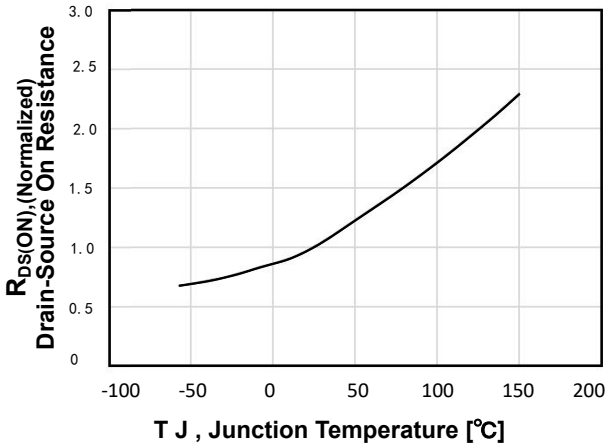


Figure 8. On-Resistance Variation vs Temperature

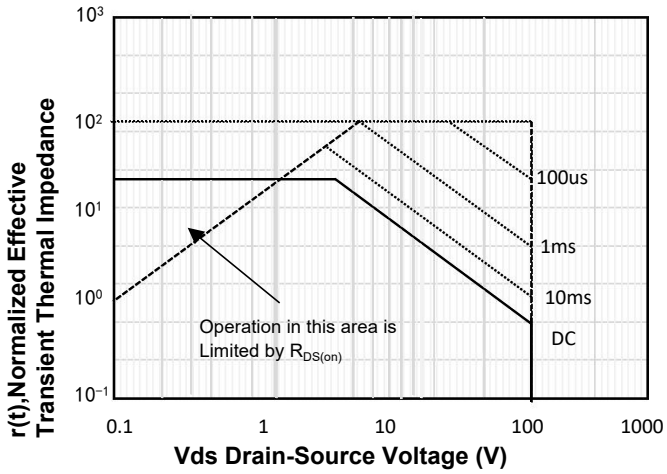
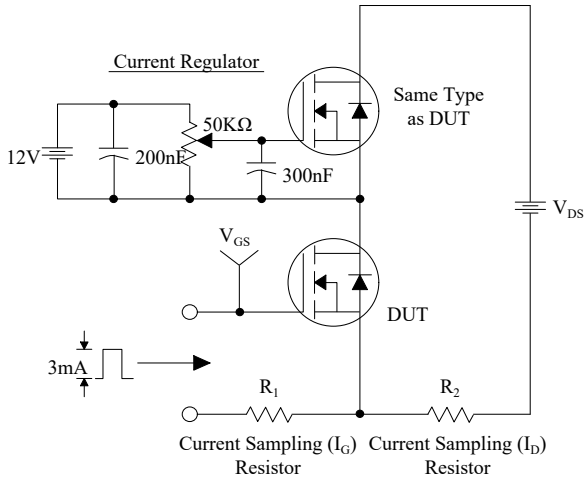
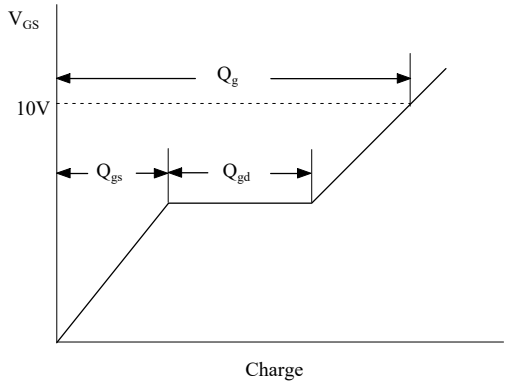


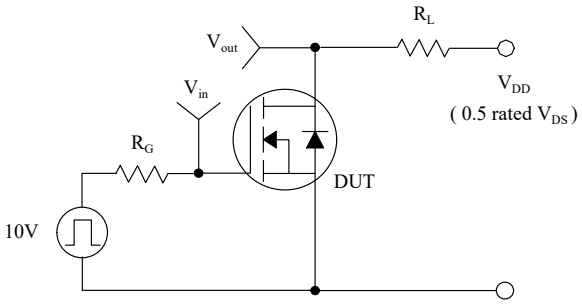
Figure 9. Maximum Safe Operating Area

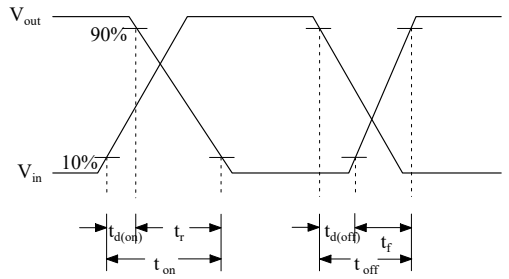
Gate Charge Test Circuit & Waveform



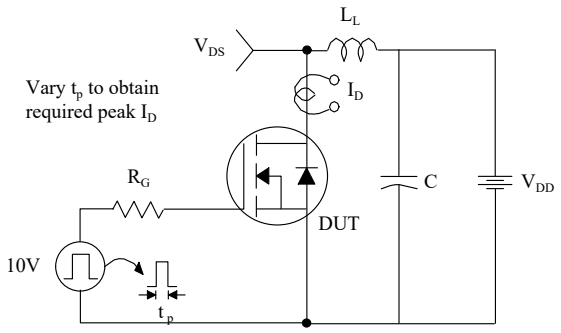


Resistive Switching Test Circuit & Waveforms

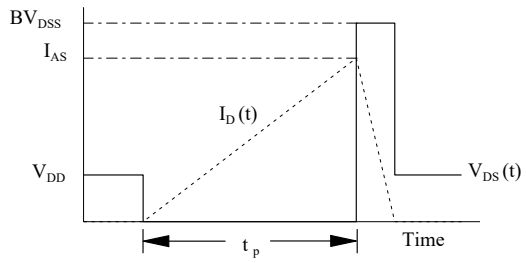




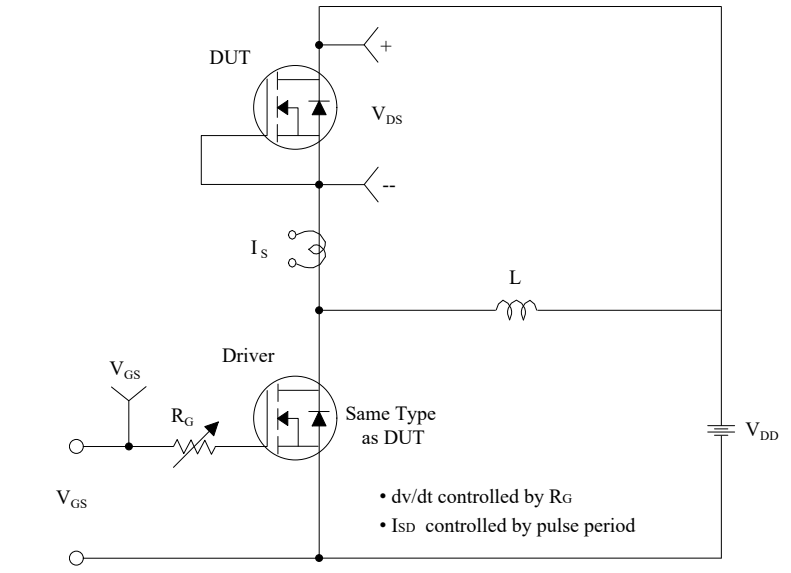
Unclamped Inductive Switching Test Circuit & Waveforms

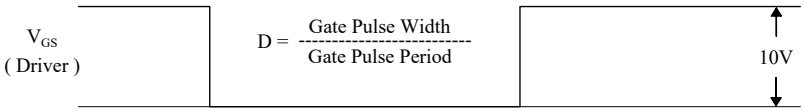


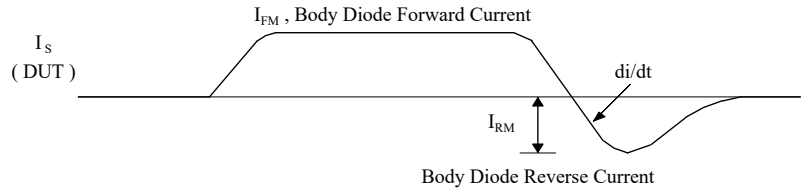
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

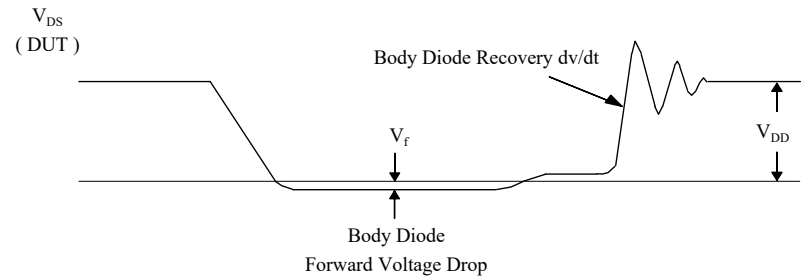


Peak Diode Recovery dv/dt Test Circuit & Waveforms

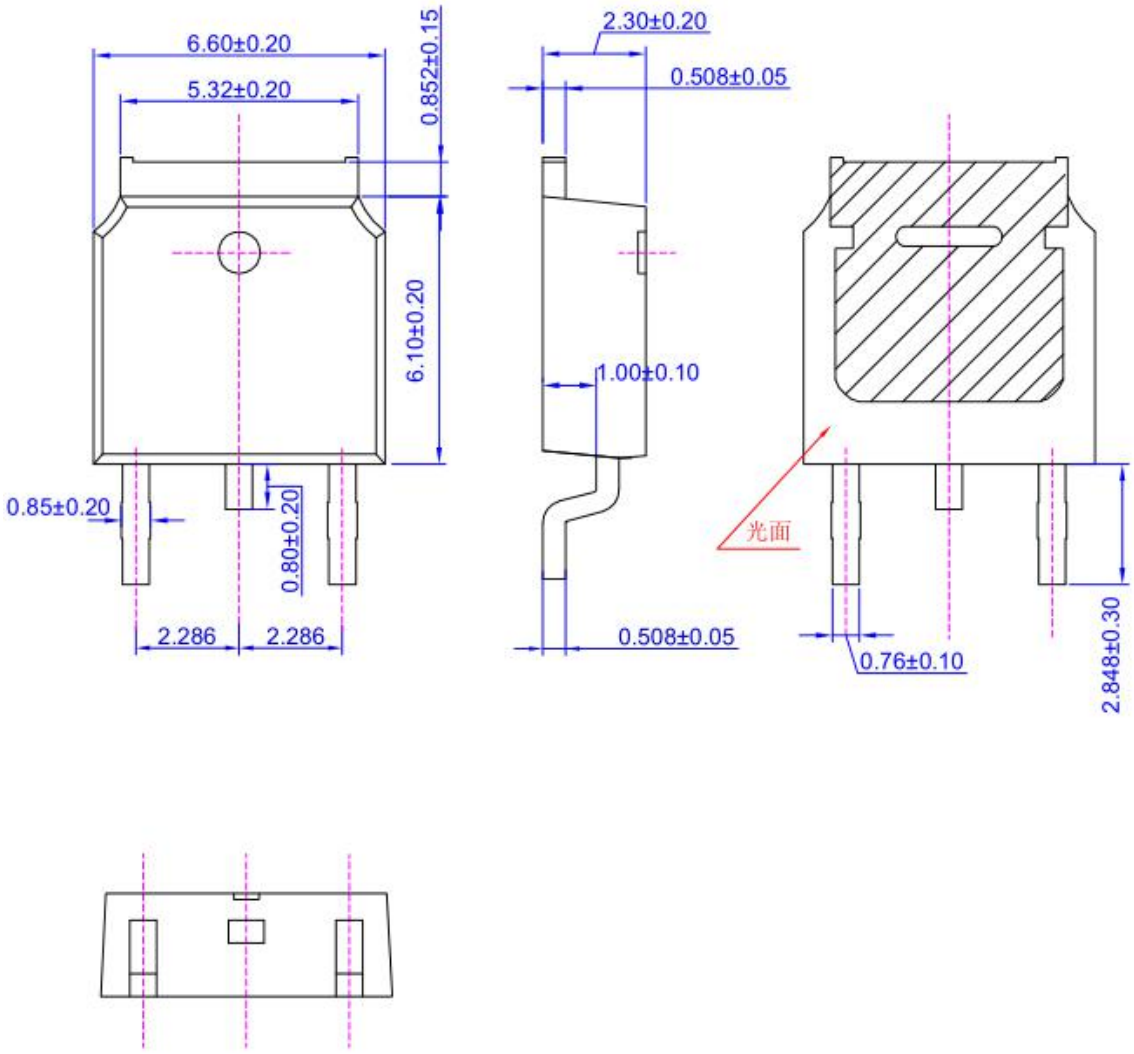








TO-252 OUTLINE



NOTE：

1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8

2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25