

SLD80N06T

60V N -Channel MOSFET

General Description

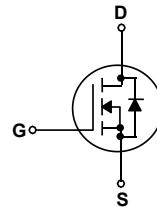
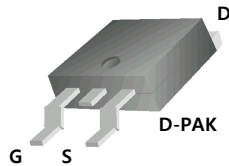
This Power MOSFET is produced using Maple semi's advanced planar stripeTRENCH technology. This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Application

- PWM Application
- Load Switch
- Power Management

Features

- N-Channel:60V 80A
 $R_{DS(on)Typ} = 5.1m\Omega @ V_{GS} = 10V$
- Very Low On-resistance RDS(ON)
- LowCrss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	SLD80N06T	Units
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$) - Continuous ($T_C = 100^\circ C$)	80	A
		52	A
I_{DM}	Drain Current - Pulsed (Note 1)	320	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy	130	mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	108	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

* Drain current limited by maximum junction temperature.

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$	--	5.1	6.8	m Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	4100	-	pF
C_{oss}	Output Capacitance		--	290	-	pF
C_{riss}	Reverse Transfer Capacitance		--	255	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V},$ $R_G = 1.8\ \Omega, I_D = 30\text{ A}$	--	9	--	ns
t_r	Turn-On Rise Time		--	7	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	38	--	ns
t_f	Turn-Off Fall Time		--	16	--	ns
Q_g	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 30\text{ A},$ $V_{GS} = 10\text{ V}$	--	91	--	nC
Q_{gs}	Gate-Source Charge		--	9	--	nC
Q_{gd}	Gate-Drain Charge		--	17	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	80	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	320	A
V_{SD}	Drain to Source Diode Forward Voltage, $V_{GS} = 0\text{ V}, I_{SD} = 30\text{ A}, T_J = 25^\circ\text{C}$	--	--	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J = 25^\circ\text{C}, V_{DD} = 30\text{ V}, V_G = 10\text{ V}, R_G = 25\ \Omega, L = 0.5\text{ mH}, I_{AS} = 23\text{ A}$
3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 0.5\%$

N- Channel Typical Characteristics

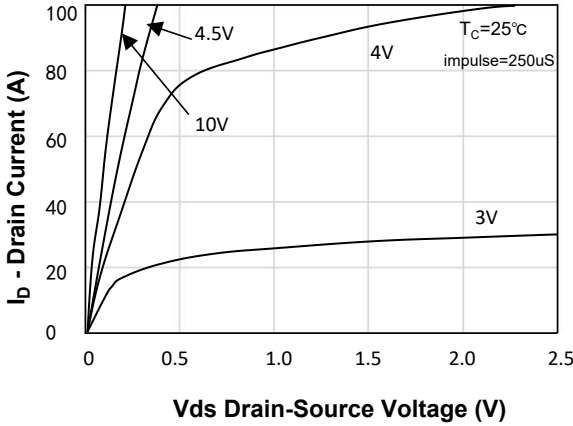


Figure 1. On-Region Characteristics

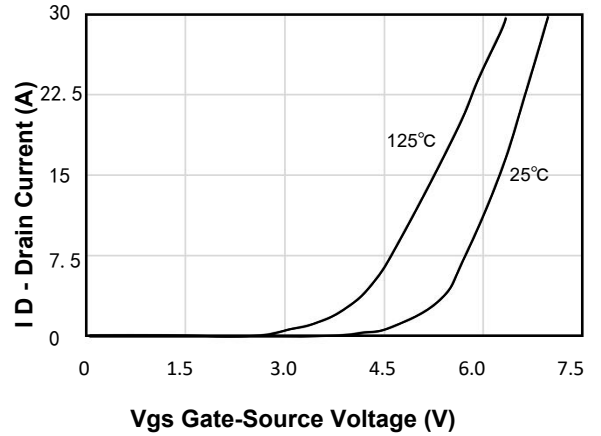


Figure 2. Transfer Characteristics

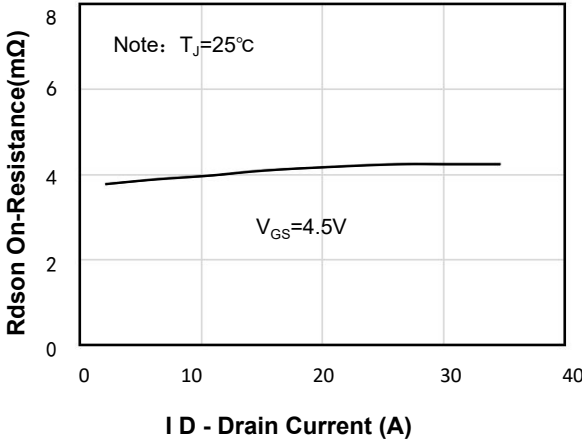


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

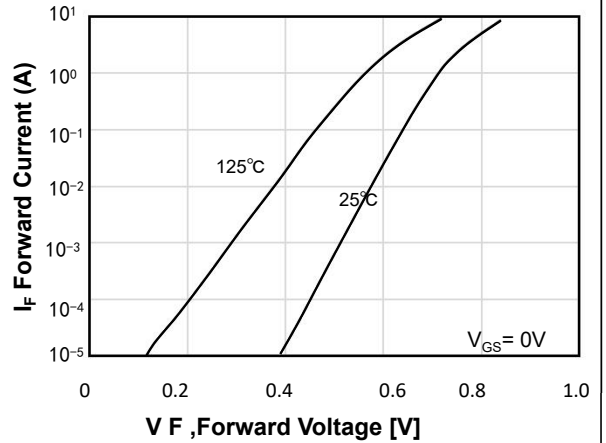


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

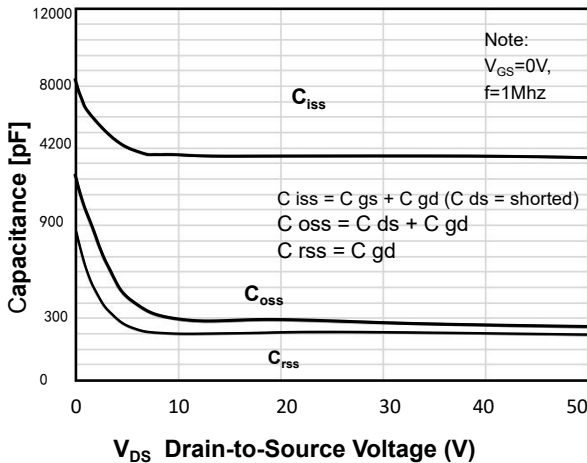


Figure 5. Capacitance Characteristics

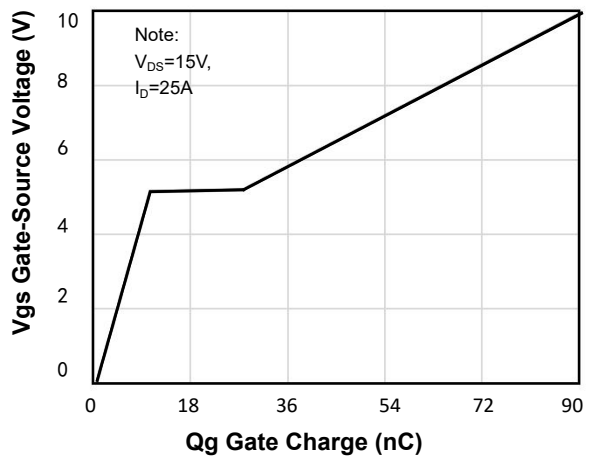


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

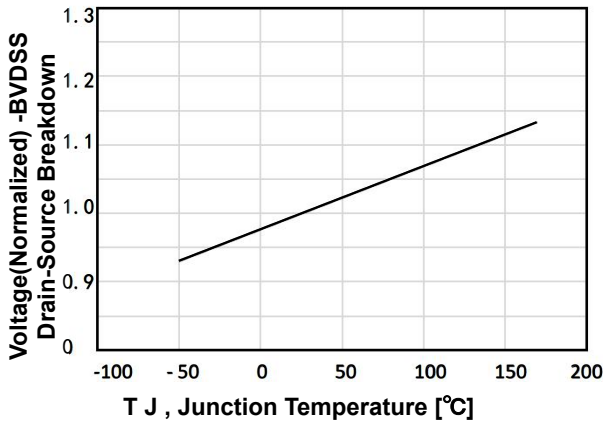


Figure 7. Breakdown Voltage Variation vs Temperature

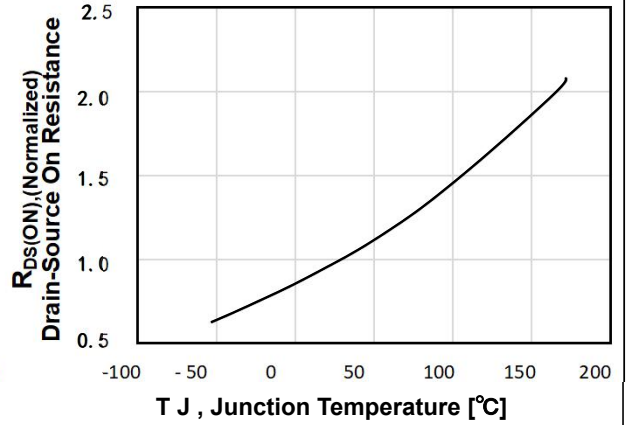


Figure 8. On-Resistance Variation vs Temperature

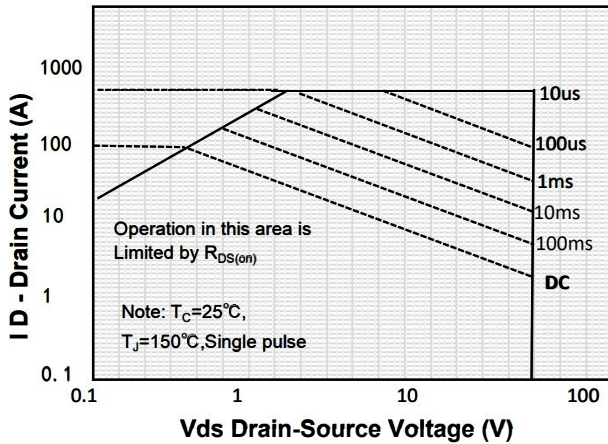


Figure 9. Maximum Safe Operating Area

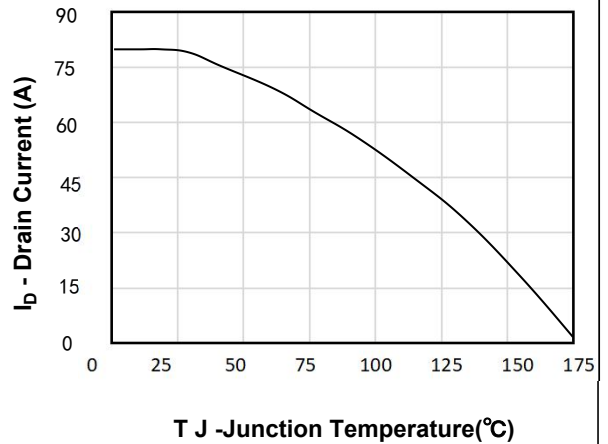


Figure 10. Maximum PContinuous Drain Current vs Case Temperature

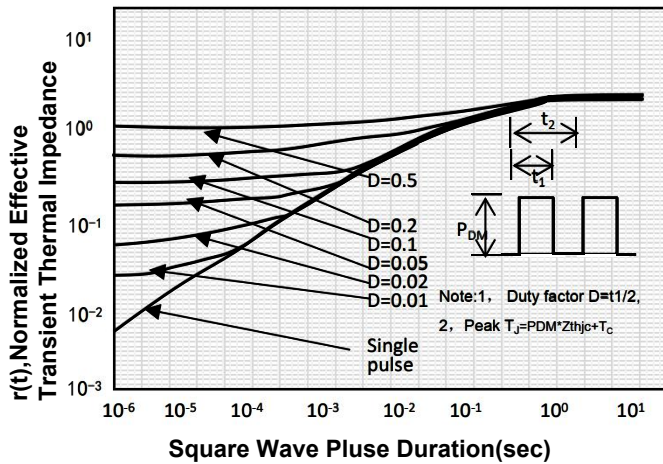
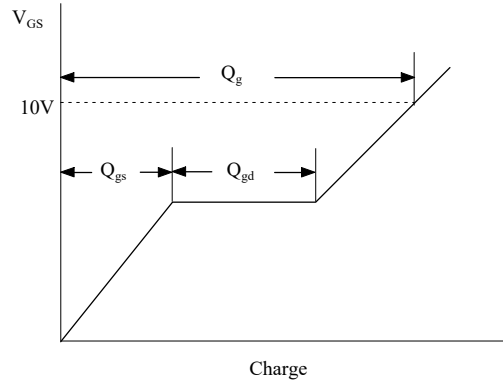
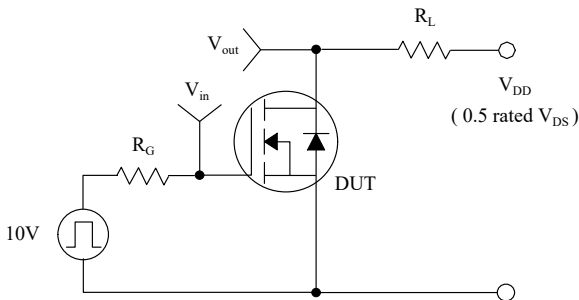


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



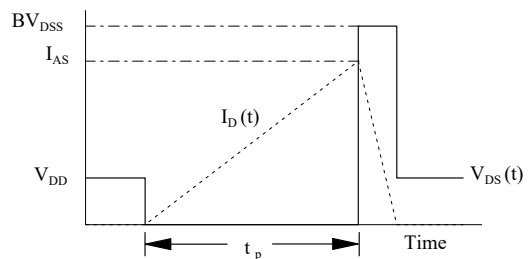
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms

